Service
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Circuit Description

Contents

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1. Introduction

Contents

One of the problems still currently experienced with television receivers is surface flicker. Surface flicker is caused because the repetition frequency of television receivers (50 Hz) with large bright surfaces (in particular when seen out of the corner of the eye) is visible to the human eye. The effect is a problem particularly with larger screen sizes (and thus also with larger brightness surfaces).
The solution to this problem is to increase the frame frequency. Although an increase to, for example, 60 Hz is sufficient to make the effect invisible, in practice it is simpler to double the frame frequency. The 100 Hz receiver thus produced reproduces each picture twice in the time it takes the 50 Hz receiver to reproduce the original picture.

The FL1.1 is the first mass-produced 100 Hz receiver.
With the FL1.2 Philips is taking another step towards higher definition television: the 16/9 (wide screen) TV receiver.

Chassis FL1.1 is suitable for the control of a 21", 25", 28" or 33" 100 Hz picture tube; chassis FL1.2 is intended for the control of a 36" 16:9 100 Hz picture tube. Units with a FL1.2 chassis are only produced in the symmetric version with separate mid-range and treble speakers.
When reading this description you will come across a number of circuits which have already been covered in the description of FL1.0 (4822 727 18238).
Of course, ample attention is paid to the new circuit parts.

In this description the circuits of chassis FL1.2 are described. Any differences with chassis FL1.1 are indicated where applicable.
For the diagrams and PCB layouts, see the service manual FL1.1 AA or FL1.2 AA.

2 Control

Contents

The control of sets having a FL1.1/FL1.2 chassis consists of a control panel which houses a microprocessor, an external ROM IC (with system software), an external RAM IC and a few LATCH ICs for the control of inputs and outputs.
This control panel is connected to the chassis via a 40-pin socket (on the small signal PC board). After the set is switched on with the mains switch (hardware reset), a test programme is started before the control programme. During the test programme all internal and external RAMs are tested as well as all circuits connected via the I^2C bus.
If a fault is detected, it will be indicated by a combination of LEDs which light up on the control panel.
In the case of an error message the LEDs flash to indicate the difference with normal use.
The inputs and outputs may be used for: RC5 reception, keyboard sensing, stand-by, anti-plop, crispening, status signals, etc.

The control in the FL1.1/FL1.2 has been designed in such a way that the functions which are used daily are directly accessible, and the functions which are used less frequently can be operated via a menu. A menu is a table with a number of options (max. 5 per table) that can be displayed on the screen.
The desired option can be selected by means of the coloured keys (red = a, green = b, yellow = c, blue = d, white = e) on the remote control and then adjusted or activated with the + or - keys of the menu part.
Several menu screens are normally needed for the operation of one function.

On the local keyboard, volume +/- and programme +/- are the only functions that are directly accessible.

On the remote control unit the following functions are directly accessible: volume +/-, programme +/-, -/-- digit entry, mute, personal preference (PP), stand-by, OSD on/off and furthermore all PIP and teletext functions and a selection of VCR functions.

2.1 Control menus

For the functions that are used less frequently the FL1.0 has 4 menu inputs of which only the main menu is accessible via the remote control.
The 4 menus are:

1) the language menu,
2) the installation menu,
3) the main menu,
4) the service menu.

For the operation of the language-, installation- and main menu see the direction for use or the diagramms in the service manual.

The service menu

This menu is used in the factory to store the characteristic data of a set (multi B/G, only UHF, PIP, NICAM, etc.). The service menu is switched on by connecting pins S23 and S2 on the small-signal panel briefly with each other.
In the Service Mode the following menu appears in the picture:

SERVICE "YY-MM-DD"		
a	Option 1	026
b	Option 2	016
c	Green	040
d	Bleu	039

In this menu "YY-MM-DD" is the release date of the softwa which is present in the set. The desired adjustment can be selected with the aid of menu keys a, b or c on the remote control.
When the "PP store" key on the local keyboard is pressed, the adjusted values are stored in the memory and the Servic Mode is left.

If the service menu does not appear on the screen, the parental mode may have been activated (it must not be activated).
By pressing the <STORE PP> key on the local control pane the data are stored and the menu screen disappears.

2.2 Service default mode

This mode has been designed for measuring or test purpose and is activated by interconnecting briefly the pins S24 and S25 (on the small signal PC board) in the set.

If this does not bring you in the service default mode, the parental mode may have been activated (it must not be activated).
When this mode is activated, the set will be tuned automatically to a frequency of 475.25 MHz (system I for UK, system L for the French-multi and system B/G for all other multi sets). All linear functions for picture and sound are set to mid-position (except for volume, which is set to low). However, as the set can still be operated normally, these settings may be changed.

SERVICE
00 <-- 00 <-- 05 <-- 06 <-- 05

Upon activation, not only the word "SERVICE" is displayed, but also 5 two-digit numbers which indicate the last 5 error messages detected by the control.
These last 5 error messages are stored in a shift register. Th five numbers may be identical, caused by an intermittent fault.
If the menu is exited by means of the <STAND-BY> key, the buffer containing these 5 last error messages will be cleared.

1.1 Block diagram

Figure 1.1 shows the block diagram of this FL1.2 television receiver. For each block see the section in this description which describes the circuits used.

The input signals are supplied via the antenna connection (terrestrial) or via the euroconnector (scart) connections. In the front-end (channel selector/intermediate-frequency combination) the high-frequency antenna signals are demodulated and converted into CVBS audio signals. The sound demodulation also takes place here. The sound signals go to the stereo decoder, after which they are supplied to the source selector switch. NICAM sound demodulation takes place on units with NICAM.

After the source selector switches, the audio signals go to the audio signal processing unit (IC/bass/treble/balance, etc.), before continuing to the sound output amplifiers and surround sound output amplifier.

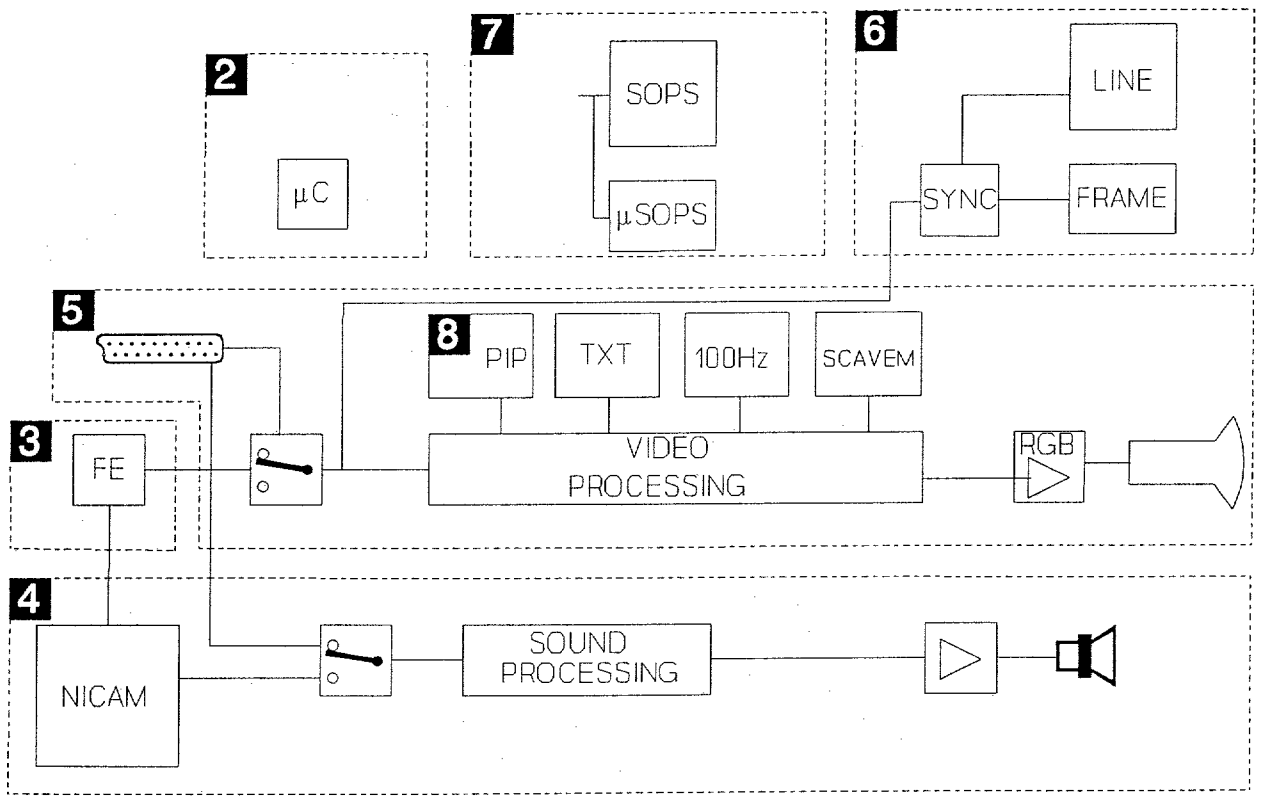


Fig. 1.1

The video signal selected continues to the video signal processing unit. Here the PIP picture is generated, Teletext acquisition takes place, 100 Hz signal processing and (for chassis FL1.2) extra SCAVEM. SCAVEM stands for scan velocity modulation; here the white to black transitions of the picture are accelerated, which results in a sharper picture. The RGB output signals go to the picture tube via the RGB amplifiers on the picture tube panel.

The operating unit controls the whole system. Operating commands may be given via the local keyboard or via the remote control. The various circuits of the unit are controlled via the I^2C bus.

Just as with other FL1 units, the main power supply is of the SOPS type. Here also the complete primary and secondary control circuit is on a separate module. The standby supply voltage is supplied by a separate transformer (μSOPS).

The DAF panel is in the line frequency part (in chassis FL1.2). DAF is an abbreviation for dynamic astigmatic focusing; here the focusing voltage is adjusted continuously, so that the picture is always in focus even in the corners.

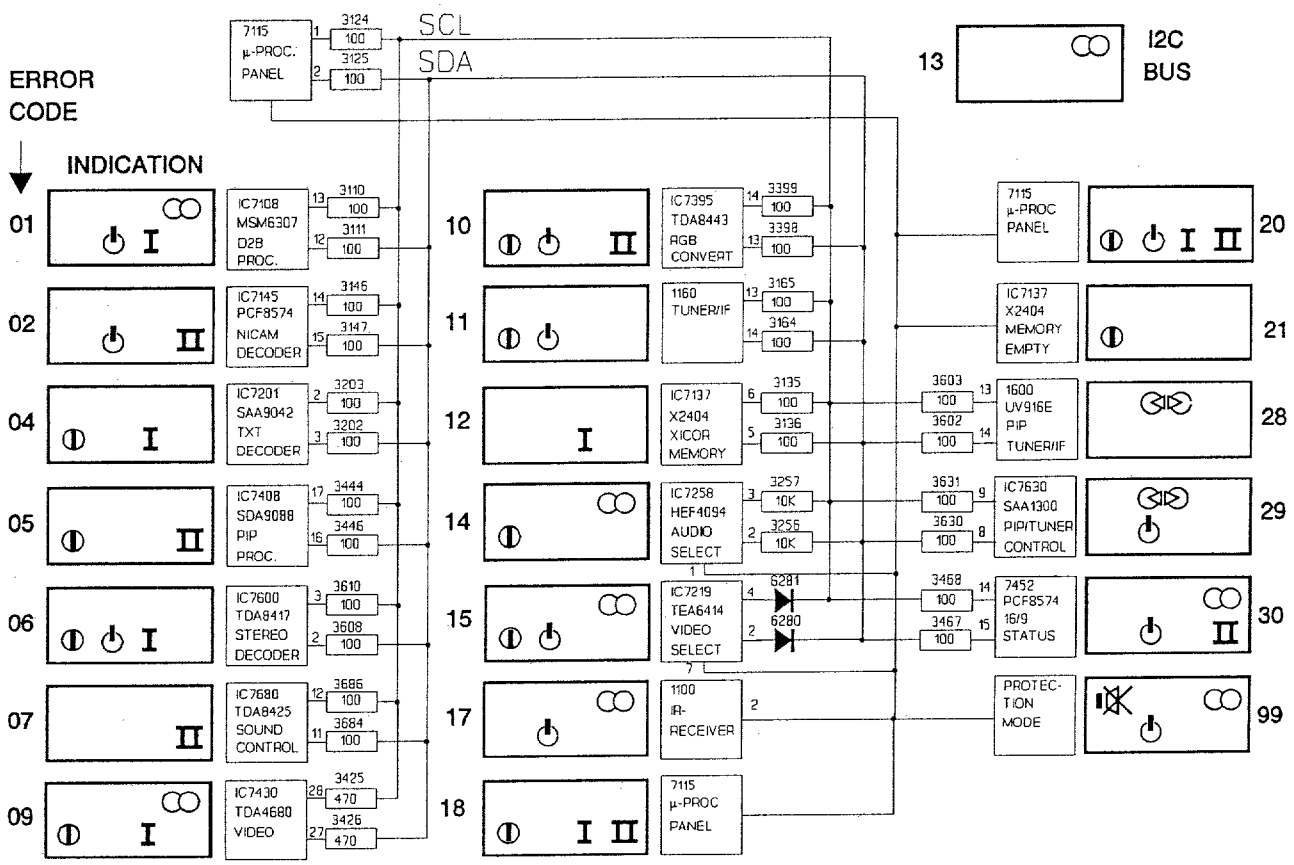
The -(R-Y) and -(B-Y) output signals of the delay lines are sent to the high-end box. The CVBS/Y signal, coming from the video source selector switch, is sent to the high-end box via a sharpness circuit, a switchable chroma bandstop filter and the adjustable delay line in IC-7324.

In the high-end box these signals are converted into video signals with a frame frequency of 100 Hz. The Y signal produced and the colour difference signals are finally supplied to IC7430 (TDA4680), the video controller, which converts the signals supplied into RGB signals. There are also separate RGB inputs for RGB signals from EXT 1 or PIP and for TXT signals. In addition, the brightness, contrast and colour saturation control, and also a cut-off point stabilisation take place in the video control IC. The sharpness of the brightness transitions is also improved by the SCAVEM panel using the Y signal.

EXT3 SVHS
The luminance signal is supplied to pin 1 of IC7219.
The chrominance signal is supplied to pin 20 of IC7219.
A CVBS signal is formed with TS7244 and TS7243 from the SVHS chrominance and luminance signals for the PIP module.

2.3 Error messages

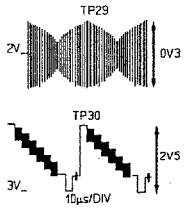
The following error messages are indicated by means of a combination of flashing LEDs and, in the "service default mode", by means of numbers.



3. The tuner / IF combination

Contents

FQ844 PAL I
FQ816/IF PAL BG
SECAM BG
FQ816ME/IF PAL BG
SECAM BGL
NTSC M
FQ816MF/IF PAL BGI
SECAM BGLL'



In FL1.1/FL1.2 4 possible tuner/IF (= intermediate frequency) combinations can be used depending of the system execution of the set. In this description the most extended version (FQ-816ME/IF) will be described.
The tuner/IF combination (front-end) consists of 2 parts, the tuner part and an IF part.

The block diagram is drawn in Fig.3.1
In the block diagram of the front-end (U1160) the following functions can be recognized.

The tuner part
The video IF circuit
The sound IF circuit

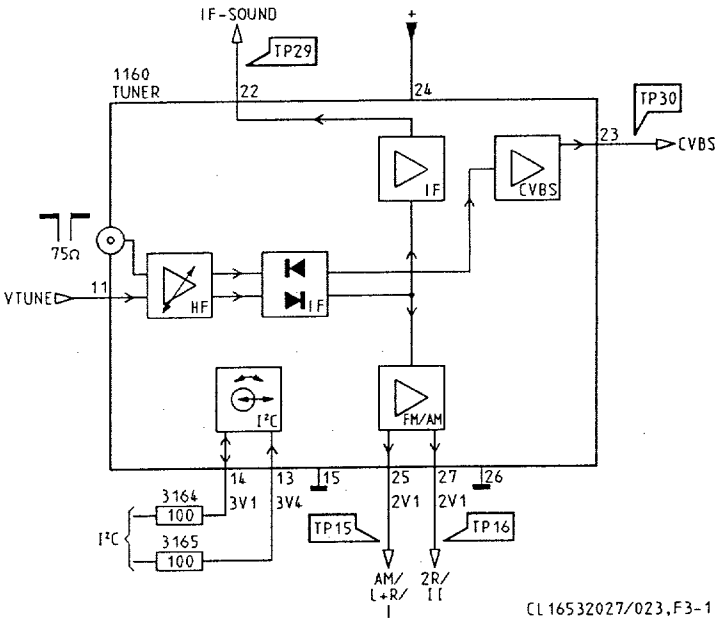
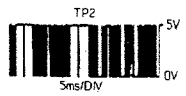


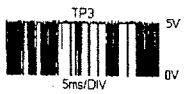
Fig. 3.1

I²C data signals

SDA (TP2)



SCL (TP3)



Voltage on pin 11 of the front-end during searching.
0V-->33V

3.1 The tuner part

The tuner used in this front-end is almost identical to the UV816 (used in chassis D16, G110, G90B etc.). This tuner is able to receive the VHF1, VHF3, UHF, S- channels but also the Hyperband, divided, internally, over 3 bands (low band, mid band and high band), see fig 3.2.

The desired band selection and tuning frequency from the control system are passed on to the channel selector via the I²C bus, pins 13 and 14. The channel selector includes a PLL (Phase Locked Loop) circuit which provides the tuning.

The tuning voltage is derived directly from the + 141V, main supply voltage. If one measures at pin 11 of the front-end a voltage between 0 and 33 V is present. This is dependent of the frequency. When searching is activated the voltage at pin 11 increases.

3.2 The IF circuitry

The IF signal (see fig 3.2) from the tuner part of the front-end enters first the audio demodulator and video demodulator.

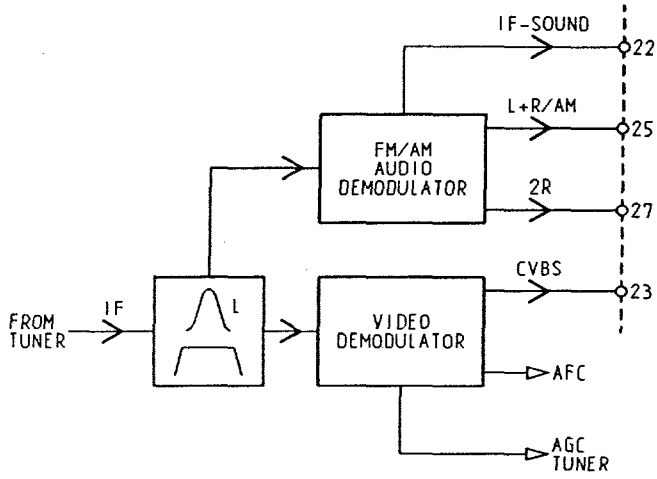


Fig. 3.2

In the audio demodulator first the IF spectrum is converted back to a frequency of 4.5, 5.5, 5.74 MHz etc, dependent of the received system. This signal is also available on pin 22 (TP 29) of the front-end where it will be used for demodulation in case of NICAM and SECAM D/K. The NICAM demodulation takes place on the NICAM module. SECAM D/K modulation takes place on te small signal panel.
AM sound demodulation, FM 4.5, 5.5 and 5.74 MHz demodulation takes also place in this audio demodulator The low frequent, still matrixed, AM / L+R signal (TP 15) leaves the front-end at pin 25 and the 2R signal (TP 16) leaves the front-end at pin 27.

In the video demodulator the IF video spectrum at 38.9 MHz is demodulated. The CVBS output is fed directly to the output pin 23, (TP30).

The information on pin 23 (CVBS out) is also used to mute the sound in case of no CVBS.
Video recognition takes place "normal" via the synchronisation IC, IC7400, see chapter 6.

4 The sound path

The following sound signals may be presented from the front end (chapter 3):

- LF AM demodulated sound (SECAM L/L')
- LF FM demodulated (matrixed) sound
- IF signal with 5.85MHz (PAL B/G) or 6.552MHz (PAL I) NICAM sound.

Stereo decoder TDA8417 and control amplifier TDA8425 have been inserted for sound processing. Two separate circuits have been added for source and record selection and a NICAM module has been added for the countries where digital sound (NICAM) is transmitted. These circuits as well as the headphone amplifier are situated on the small signal PC board.
The output amplifiers are housed on the large signal PC board.

4.1 Sound processing

(Figure 4.1) see page 4.13

Stereo decoder

The two FM demodulated LF signals 2R (TP16) and L+R (TP15), originating from the TUNER/IF combination (Front-end), are supplied to stereo decoder IC7600 (TDA8417).
The status (MONO, DUAL LANGUAGE or STEREO) is determined in the stereo decoder. Depending on the status, the control microcomputer sets the de-matrix circuit in the correct position via the I^2C bus.
With dual language broadcasts the language selected is sent on to the source/record selector circuits and to euro-connector 1.

AM sound

With SECAM L/L' broadcasts the AM demodulated LF sound is fed to pin 9 of the stereo decoder (IC7600).
For SECAM L/L' this sound source is selected via the I^2C bus.

NICAM

If a NICAM module is present, the IF signal with digital sound (TP29) coming from the front-end is fed to the NICAM module (U1600).
On the NICAM module the digital sound is bypassed and converted into an analog signal.
If no digital sound is present in the IF signal, this will be detected on the NICAM module and the system will switch over to analog (FM) sound. The analog sound comes from the stereo decoder.
In this case the sound signals to euroconnector 1 come via a buffer (IC7193) from the NICAM module outputs.

Source/record selection

The sound signals (TP19 and TP20) travel to the SOURCESELECT circuit (IC7620, HEF4052) and to the RECORDSELECT circuit (IC7622, HEF4052).
There a choice is made between the sound signal from the stereo decoder (or NICAM module) or from one of the EXTERNAL sound sources (EXT1, EXT2 or EXT3).

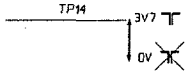
Control amplifier

The sound source selected in IC7620 is fed via a buffer circuit (IC7630, LF353) to the AGC amplifier (IC7680, TDA8425).
In the AGC amplifier the BASS, TREBLE, VOLUME, BALANCE, SPATIAL and PSEUDO functions and the MONO/STEREO switch are controlled via the I^2C bus.

The sound signals (TP8 and TP9) continue on their way to the sound output amplifiers, which are located on the large signal PC board.
A separate amplifier takes care of the sound for the headphones. This amplifier is located on the small signal PC board.

Mute

From the CVBS signal originating from the front-end a mute voltage is made, which is supplied to pin 18 (mute input) of the stereo decoder (see Fig. 4.2.).



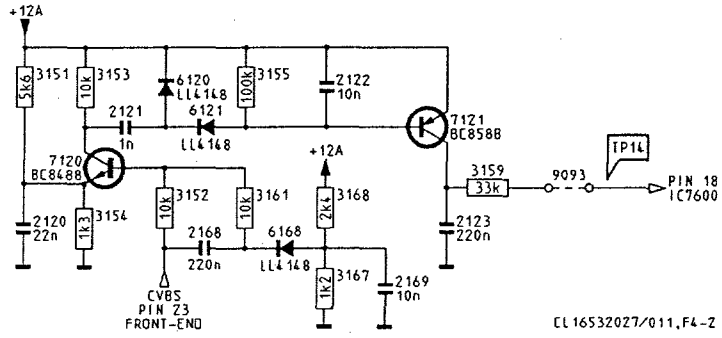
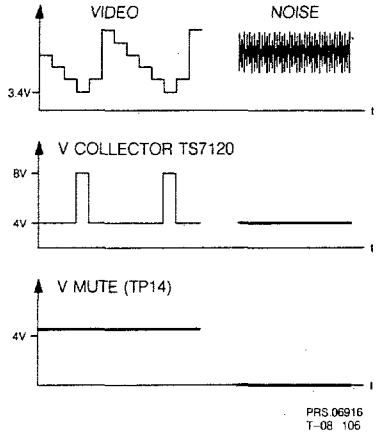


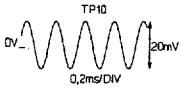
Fig. 4.2

If video present:
The CVBS signal is supplied to the mute circuit. This circuit removes the sync pulses from the CVBS signal and rectifies them to a DC voltage of 5V (TP14).
Now sound is present at outputs 11 through 14 of the stereo decoder.

No video present:
If no video is present, no sync pulses are detected. The output voltage then is 0V (TP14) and the sound is muted at all outputs (11 through 14 of the stereo decoder).



Headphone amplifier



This amplifier consists of two parts: an amplifier (IC7704) and a current amplifier (TS7706, TS7708). (see Fig. 4.3)

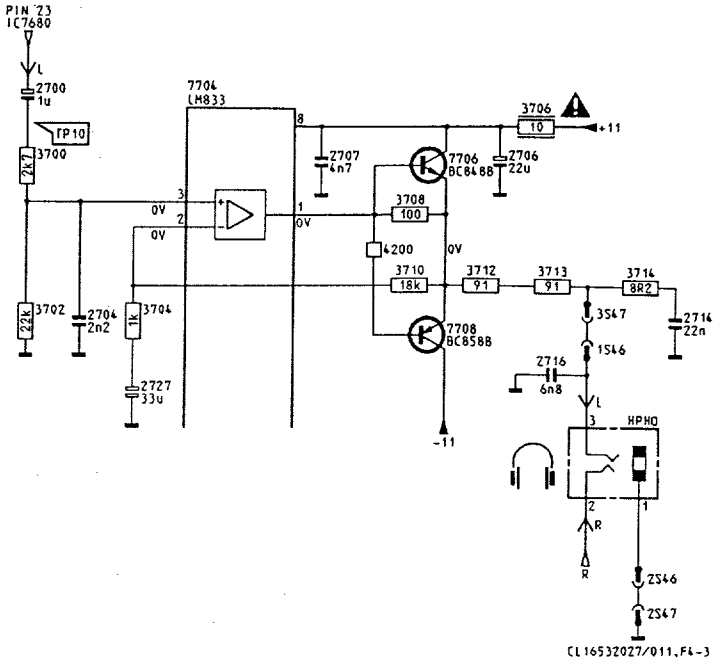


Fig. 4.3

The voltage gain is determined by feedback circuit R3710, R3704 and C2727. The gain factor for the low frequencies is smaller because of the presence of C2727 in the feedback circuit. The amplified sound signal then goes via the emitter follower, built up of transistors TS7706 and TS7708, to the headphones.
With small signals the current flows via R3708, R3712 to the headphones to prevent distortion and oscillation.
When the mute button on the remote control is pressed, the sound on the headphones is not affected.

4.2 The NICAM sound path

The NICAM IF signal is supplied to the NICAM input bandpass filter (1106) (see Fig. 4.4). This filter has a response frequency of 5.85 MHz for PAL BG or 6.552 MHz for PAL I. The NICAM phase-modulated sound signal remaining after filtering (PM sound) goes to pin 4 of the QPSK demodulator TA8662.

The QPSK demodulator

This circuit (see fig. 4.4) converts the phase-modulated carrier wave into a serial bit stream which again complies with the NICAM format. The filtered phase-modulated signal is supplied to the AGC circuit. The output signal of the AGC circuit is supplied to the QPSK demodulator. The output signals of this demodulator are taken to the outside via pins 10 and 11. These signals are filtered by the low-pass filters L5124/C2124 and L5125/C2125. Via pins 20 and 19 the filtered data signals are supplied to the phase detector of the internal oscillator. The type of crystal in the reference circuit depends on the system and is 6.552 MHz for PAL I and 5.85 MHz for PAL BG.

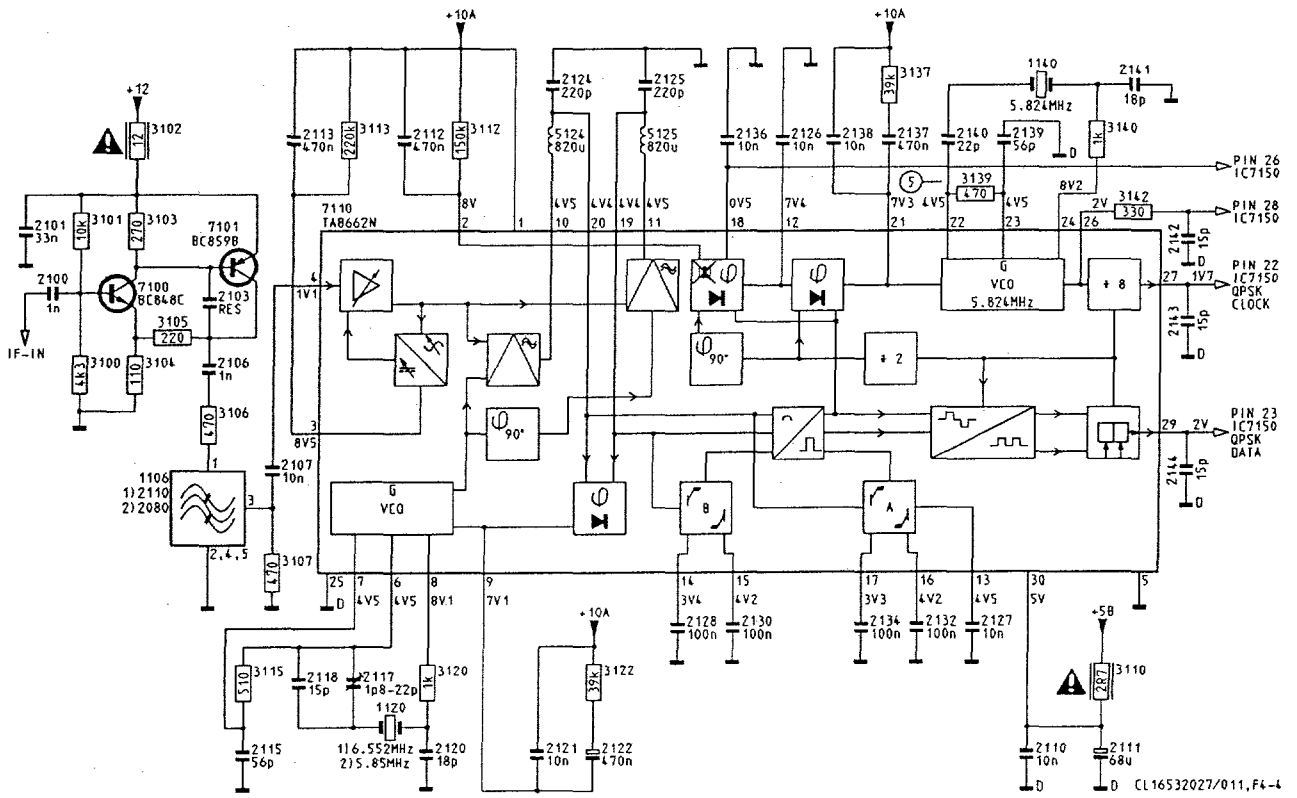
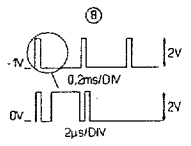


Fig. 4.4

The filtered data signals then continue to the differential encoder circuit. Via a 2-bit parallel/serial converter the NICAM coded signal at pin 29 is taken to the outside. Pin 18 is the output for the NICAM mute signal.The 5.824 MHz clock signal is available at pin 24 and the 728 kHz clock signal at pin 27.

The NICAM decoder (CF70123)

Service tip
Using the colour pattern generator PM5515TN, PM5518TN or PM5518TNI, the QPSK demodulator and the NICAM decoder can be tested.
When test signal DATA1 is used, a pulse train can be measured at pin 29 of the QPSK demodulator. In this situation the NICAM decoder will also give a pulse train at pin 8 (ERFL). The DATA2 test signal is used to test the NICAM decoder. In this situation a 32 kHz pulse train can be measured at the I²S bus.
The DATA3 test signal gives an unmodulated NICAM sound carrier wave which is used for settings.



The NICAM decoder ensures that the serial digital information, coded according to the NICAM system, is converted again into 14-bit words which can be processed directly by a D/A converter (see fig. 4.5).

The data signal comes in at pin 23 and is read in using the clock signal at pin 22. (The data signal of the QPSK demodulator is locked to the clock signal). The read-in signa is first descrambled. The descrambled data are taken to the outside via pin 7. The data signal at pin 7 is read in again directly at pin 15. The NICAM decoded signal is then converted into a signal according to the I²S format. This signal comes via pins 3, 4 and 33 from the NICAM decoder IC and goes via a digital filter, IC7165 (SAA7220), to the DAC IC7170 (TDA 1543). The NICAM control bits are present at pins 35 to 38. These control bits indicate what kind of signal is present (MONO/STEREO/2 LANGUAGES). These control bits are sent to the microprocessor via the I/C Expander (IC7145) and the I²C bus.

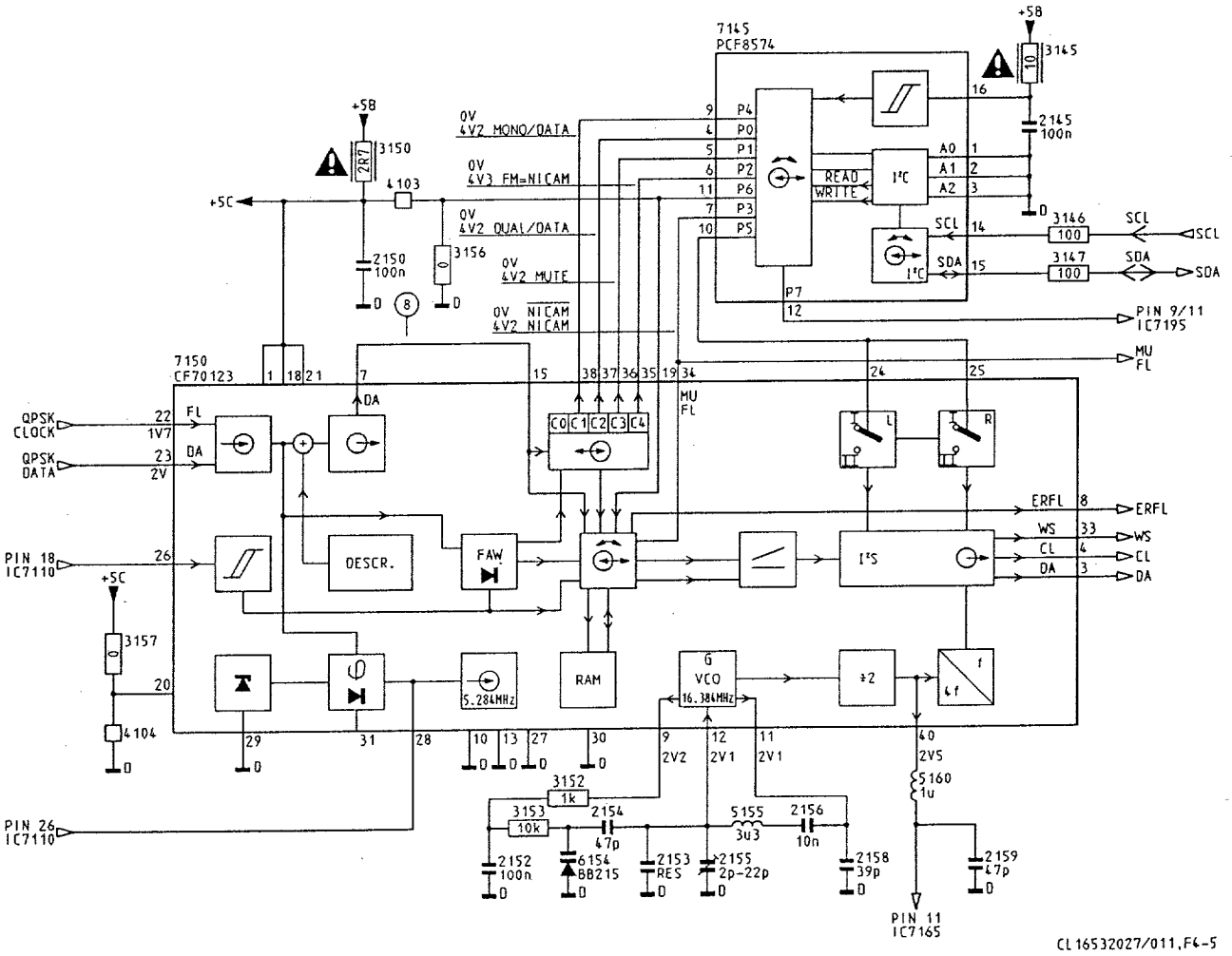


Fig. 4.5

The digital filter (SAA7220)

The I^2S signal comes in at pins 1, 2 and 3 (see Fig. 4.6). This is divided into a left and right signal.

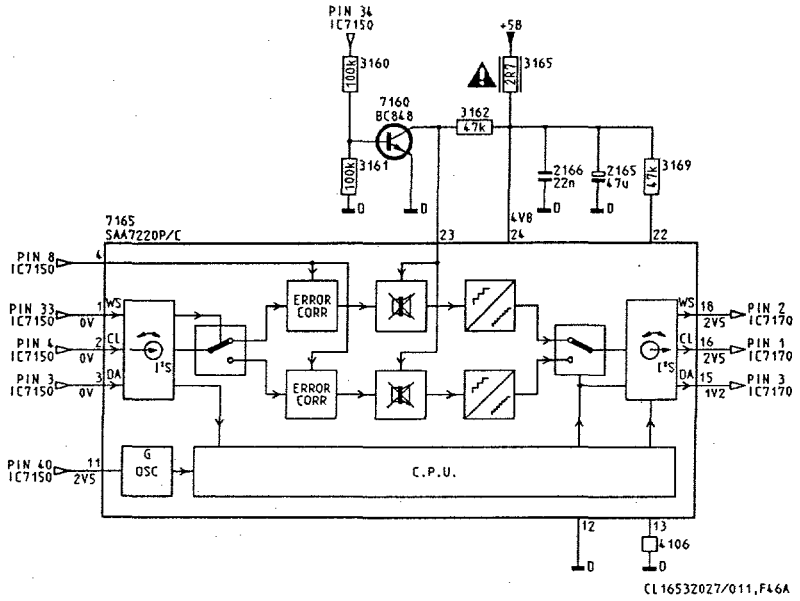


Fig. 4.6

If the Error flag (pin 4) indicates that a faulty sample is coming in, this is replaced by another sample which is between the previous and the next good sample. The signal can then be suppressed by a low level at pin 23 (mute). This is done by pin 34 of IC7150 which then makes transistor TS7160 conduct. The digital filter then converts the 32 kHz samples into 128 kHz samples. The advantage of this is that the analogue filter may have a lower order, which means that the frequency response is not affected as much. The output signal is converted into a signal according to the I^2S format and is taken to the A/D converter via pins 15, 16 and 18.

The D/A converter (TDA1543)

IC7170 (see fig. 4.7) contains an I^2S interface and two D/A converters.
The I^2S interface takes the data from the left and right channel from the I^2S signal and sends them to their respective D/A converters. These convert the samples supplied into an equivalent current at output pins 6 (left) and 8 (right). With this current a reference current is also added internally which also goes to the outside via pin 7. This reference current raises the zero level of the output signals, which improves the dynamic range. With the signal from pin 7 this current can be compensated again in the analogue filters.

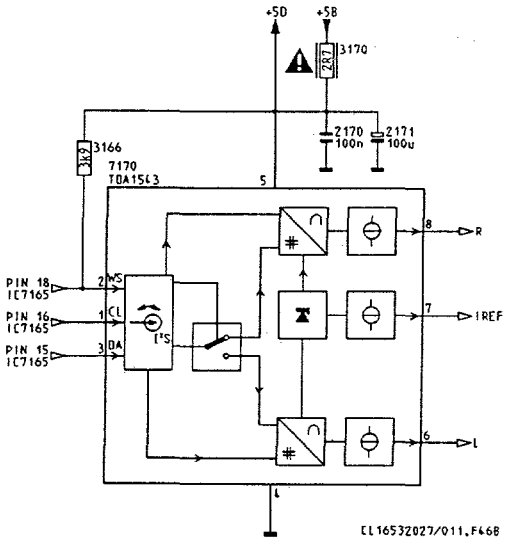


Fig. 4.7

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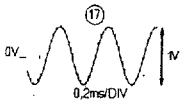
The analogue filters



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The output signals at pins 6 and 8 of the DAC (see fig. 4.8) are sent to two selective amplifier circuits.

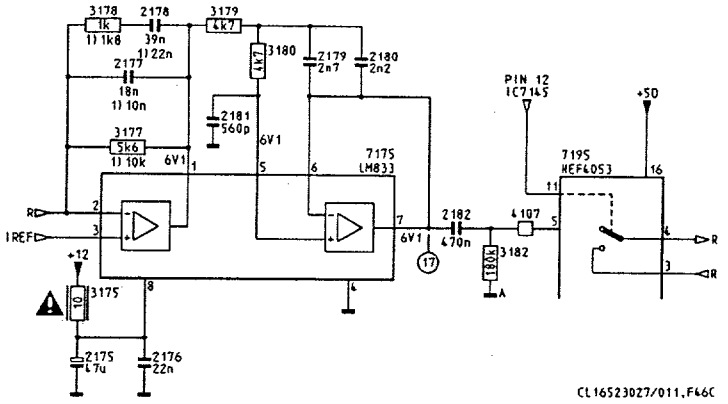
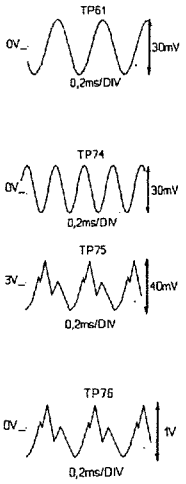


Fig. 4.8

A selective amplifier circuit consists of an operational amplifier (IC7175 or IC7185) and several passive components. The current at pin 2 (-input) is converted into ar output voltage. The value of this current is however offset with regard to the actual value because a current is added to it in the D/A converter. By supplying a direct current (from pin 7 of IC7170) at the + input (pin 3) of the operational amplifier, the offset is lifted. The L.F. sound signal is now available at pins 7 of IC7175 (right) and IC7185 (left), and from there goes to the FM sound/NICAM sound selection circuit in IC7195.

4.3 Sound output amplifiers



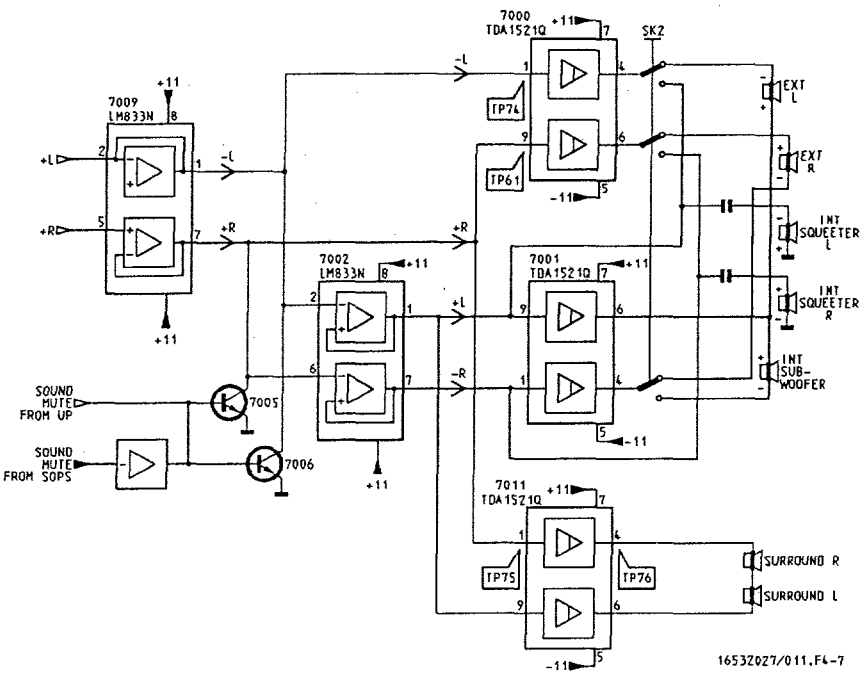


Fig. 4.9

The sound signals coming from the AGC amplifier (IC7680) are sent to a preamplifier (IC7009), where the L-signal is inverted. The R-signal is not inverted. Consequently, there is -L and +R at the output of IC7009.
These signals are supplied to the output amplifier IC7000 and a second preamplifier IC7002. IC7002 inverts both signals, so that L and -R are present at the outputs of these amplifiers. These signals are supplied to the output amplifier IC7001.
With SK2 it is possible to select between external squeeters (mid range and treble) and external full range loudspeakers. If the squeeters are selected, one SUBWOOFER (central bass system) is connected in the unit between -R and L of IC7001. This subwoofer reproduces signals up to approximately 500 Hz.

The squeeters are connected via capacitors between the -L output and earth and +R output and earth of the output amplifier IC7000.
If external loudspeakers are selected, then external FULL RANGE (low, mid and high) loudspeakers must be connected. The left loudspeaker is connected between the -L output of IC7000 and the +L output of IC7001. The right loudspeaker is connected between the +R output of IC7000 and the -R output of IC7001.

The +R output signal of IC7009 and the +L output signal of IC7002 are sent to the surround sound output amplifier IC7011. The surround sound loudspeakers are connected between the +L output and the +R output of IC7011. With stereo transmission the surround sound loudspeakers thus indicate the difference between L and R. With mono transmission (L and R equal) the surround sound loudspeakers produce no signal.

The main output amplifier

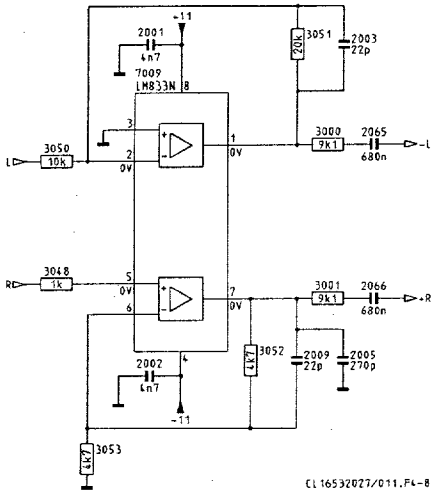


Fig. 4.10

IC7009 contains two opamps. The L signal from the control amplifier (IC7680) is controlled at the -input of one opamp. The R signal is controlled at the +input of the other opamp. In order to prevent oscillations the amplification of both opamps is doubled. The amplification is determined by R3050, R3051 and R3052, R3053 (see Fig. 4.10). Thus -2L and +2R come out of the preamplifier (IC7009). The output amplifiers in IC7000 have an input impedance of approximately 10k. The -2L and +R signals are reduced again to -L and +R by the series resistors R3000 and R3001 and taking into account the input impedance of the output amplifiers. These signals are also connected with the output amplifier IC7000 and a second preamplifier IC7002 (see Fig. 4.11). IC7002 also has 2 opamps, whose amplification is determined by R3006, R3005 and R3009 and R3004.

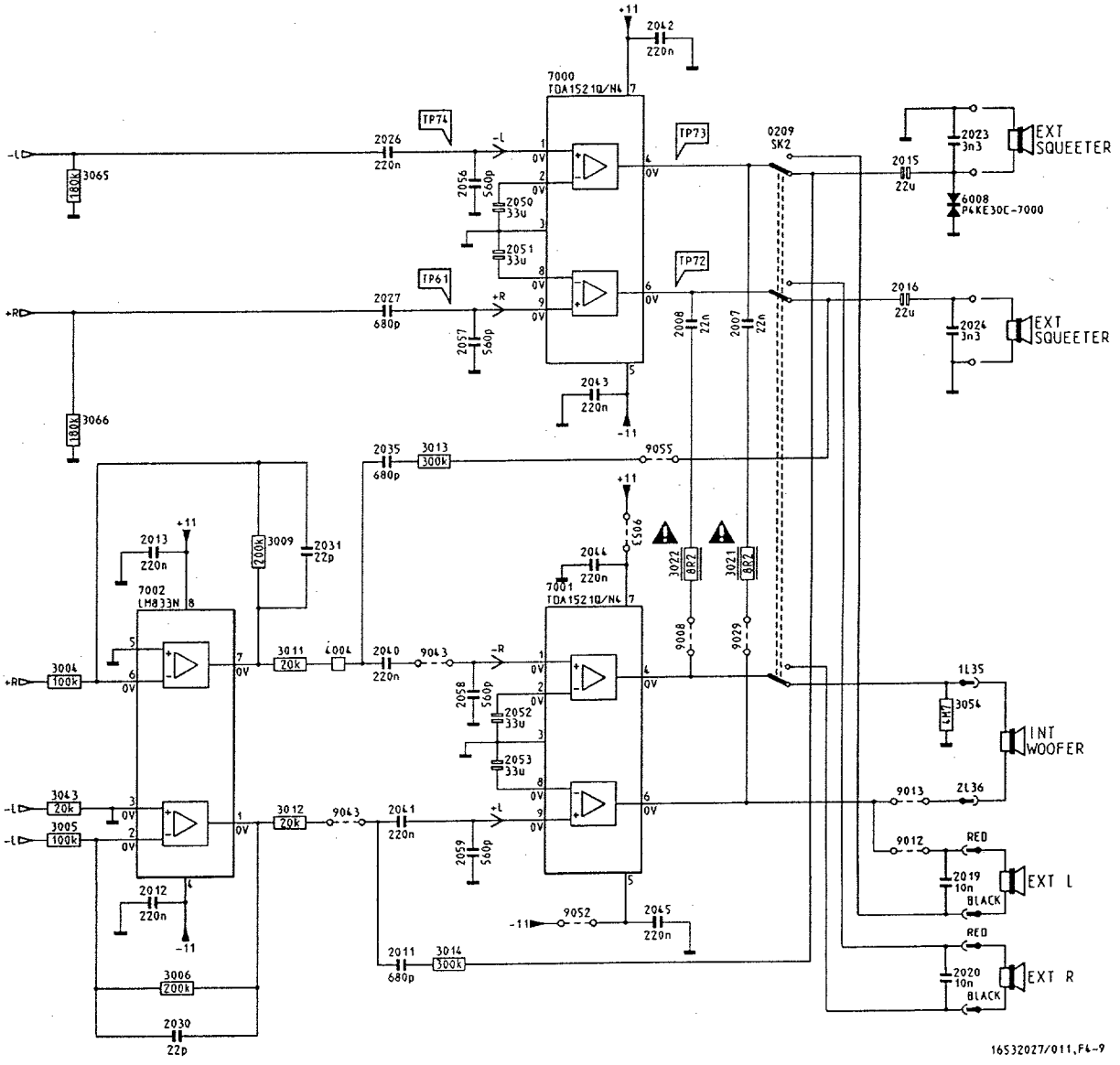
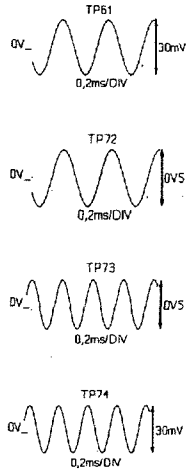


Fig. 4.11



The amplification is also multiplied by 2. Both opamps are controlled at the -input. There is thus a +2L and -2R signal from IC7002. Via R3012, C2041 and R3011, C2040 the +2L and -2R signals are also reduced once more to +L and -R signals (input impedances of IC7001), which are sent to the output amplifiers in IC7001.

The AC amplification of IC7000 and IC7001 is determined internally and is 34x.
The outputs of the output amplifier IC7001, pin 4 for -R and pin 6 for +L, are connected via SK2 (in the bottom position) to the internal subwoofer (see Fig. 4.7).

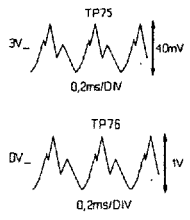
Via SK2 and R3014, C2011 and R3013, C2035, the outputs of IC7000 are fedback to the inputs of IC7001. Consequently, a frequency-dependent feedback is obtained. C2011, R3014 and C2035, R3013 allow single signals through from 500 Hz. Thus single signals up to 500 Hz remain at the input of IC7001, which means that the subwoofer only reproduces the low frequencies up to 500 Hz.

The squeeters are connected via capacitors between +R (pin 6, IC7000) and earth and -L (pin 4, IC7000) and earth. The L squeeter is connected in the opposite direction so that the +L signal is still reproduced (otherwise the squeeters would be connected in opposite phase). The frequency of the squeeters ranges from approximately 500 Hz to 15 kHz. The squeeters also produce the stereo effect, because stereo is primarily audible in this frequency range.

If the external loudspeakers are switched on (SK2 in the top position), they are connected between IC7000 and IC7001 (Fig. 4.8).

This means that the left loudspeaker is connected between -L and +L and the right loudspeaker between +R and -R. In this way the capacity with regard to the squeeters is doubled.

The surround sound amplifier



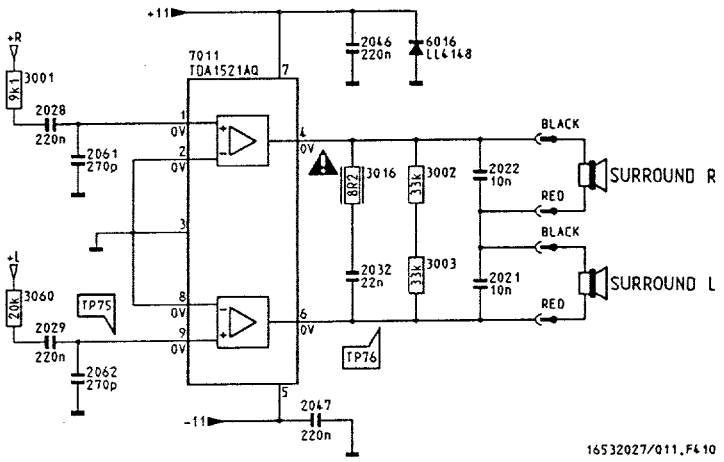


Fig. 4.12

The +L signal from the preamplifier IC7002 is supplied to th surround sound output amplifier IC7011 via R3060 and C2029 (see Fig. 4.12).
The +R signal from the preamplifier IC7009 is supplied to th surround sound output amplifier IC7011 via R3001 and C2028.
The amplification of IC7011 is determined internally and is also 34x. The surround sound loudspeakers are connected in series between pin 4 (+R) of IC7011 and pin 6 (+L) of IC7011. In this way the surround sound loudspeakers indicat the difference between L and R.

Sound suppression

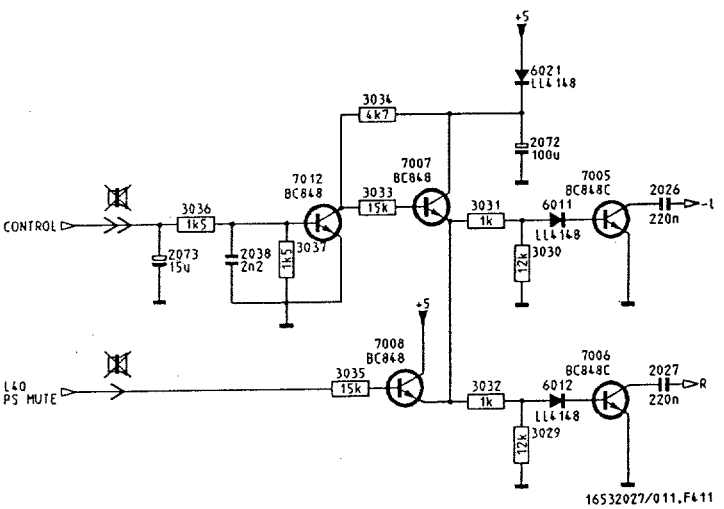


Fig. 4.13

The sound will be suppressed during switching on and off an also when the MUTE button on the remote control is operate (see Fig. 4.13).

Mute button

If the MUTE function is pressed on the remote control, the microcomputer of the operation will make the base of TS7008 high. This causes TS7005 and TS7006 to conduct and the sound is switched off.

vitching the unit off

If TS7006 and TS7005 conduct, the signal at the output of IC7009 is short circuited. The base of TS7012 is high with the SOPS power supply and low if the SOPS power supply is switched off.
If the base of TS7012 is high, then TS7012 conducts. TS7007 is thus blocked, as are TS7005 and TS7006.
If the base of TS7012 is low (SOPS supply switched off), TS7007, TS7006 and TS7005 conduct. This switches off the sound.

vitching the unit on

When starting up the microcomputer of the operation will make the base of TS7008 high approximately 250 ms high. This causes TS7005 and TS7006 to conduct and the sound is suppressed. As long as the SOPS power supply has still not started up completely, after these 250 ms the sound will remain switched off by TS7012.

C protection

An asymmetric deviation of the +11V and the -11V supply voltage produces a positive or negative potential at point A (see Fig. 4.14).

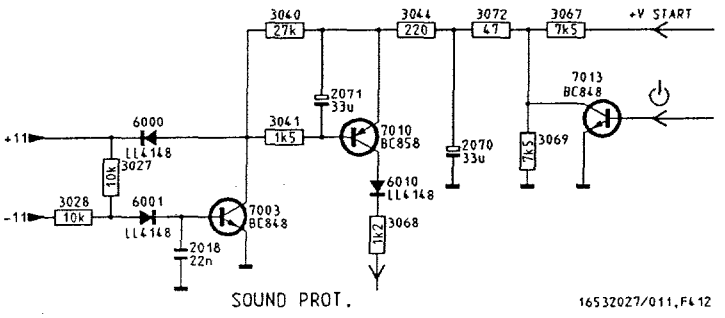


Fig. 4.14

If the voltage at point A is greater than 0.6V (D6001) + 0.6V (be-TS7003) = 1.2V, TS7003 will start to conduct and thus also TS7010, which means that the SOPS supply will be switched to protection (see § 7.1).
If the voltage at point A is less than -1.2V, TS7004 and TS7010 will conduct.
If the +11V and the -11V are short circuited with one another, D6000 conducts, with the result that TS7010 starts to conduct and the supply is switched to protection.

The supply voltage of the protection circuit comes from +V start, which comes from the μ-SOPS. This means that the supply voltage (+V start) is still present during standby mode. In order to switch the protection circuit off during standby, transistor TS7013 is added. TS7013 is made to conduct during standby via TS7385 by the microcomputer of the operation. TS7013 now short circuits to earth and the protection circuit is switched off.

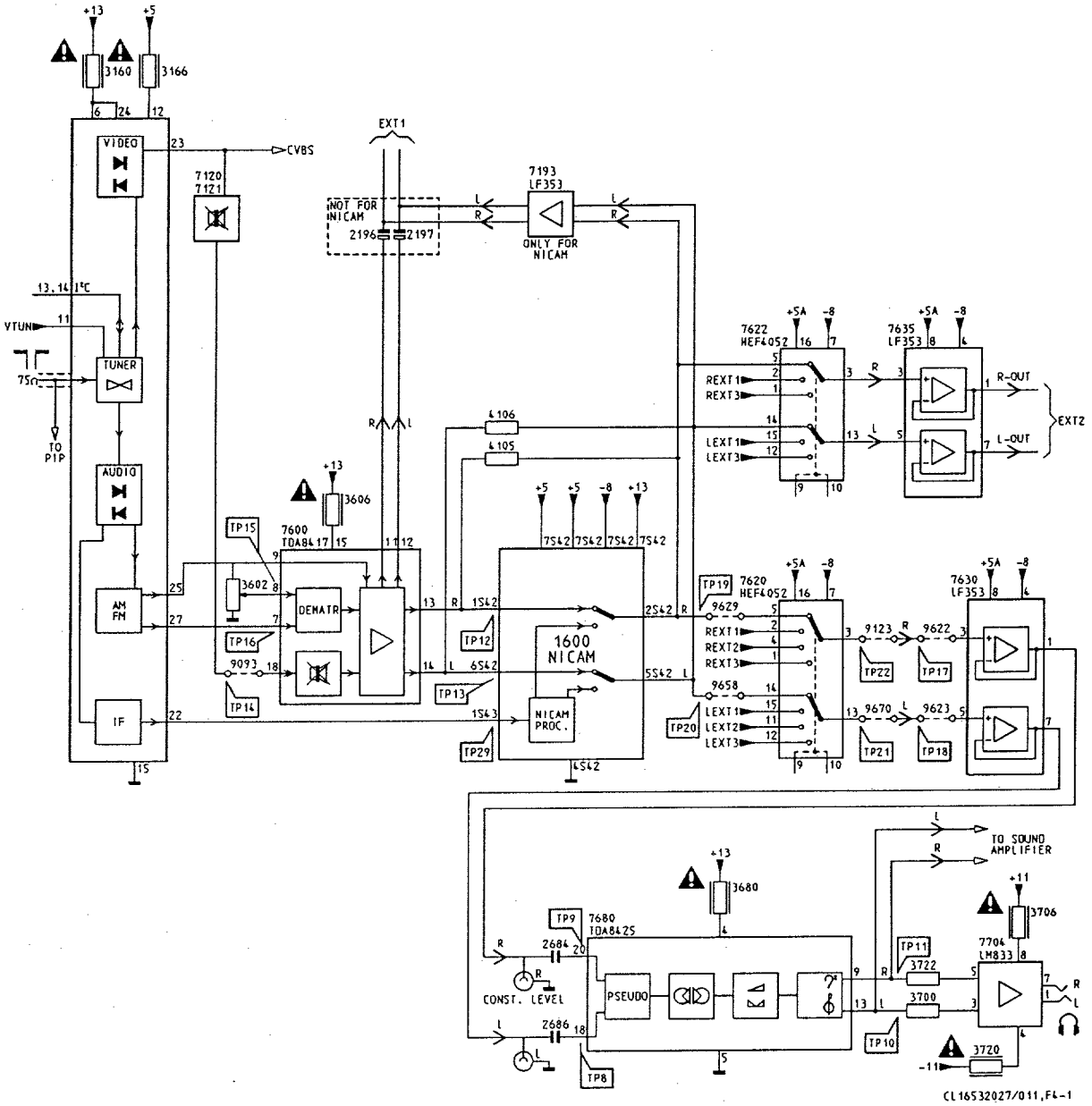
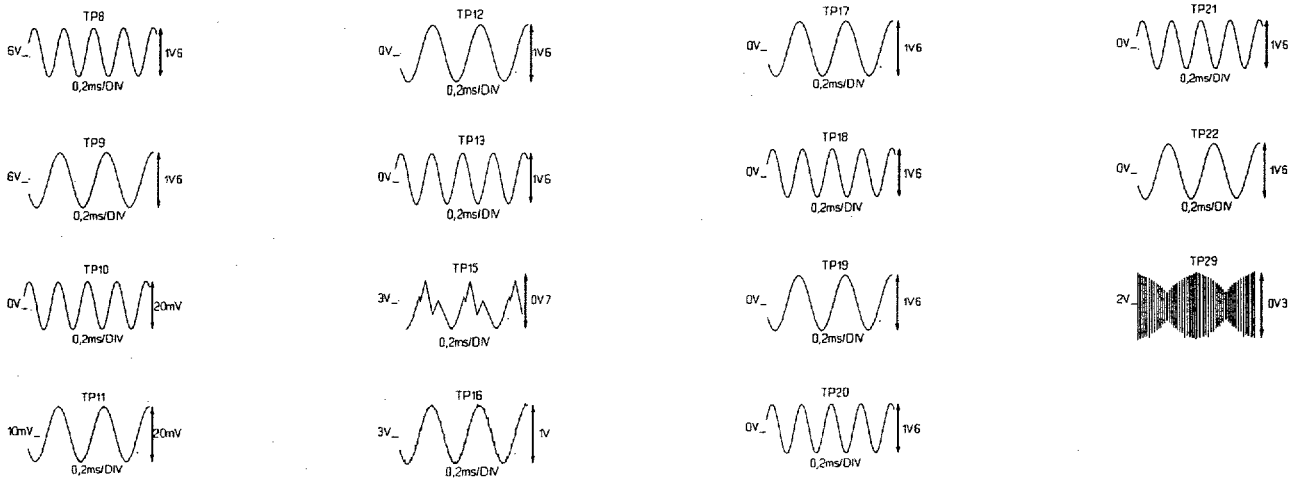

+13
+5
3160
3166
VIDEO
CVBS
7120
7121
EXT1
NOT FOR NICAM
2196
2197
7193
LF353
ONLY FOR NICAM
VTUN
TUNER
75Ω
TO PIP
AUDIO
AM FM
IF
3606
7600
TDA8417
TP15
3602
DEMATR
TP16
9093
TP14
TP12
TP13
1600 NICAM
NICAM PROC.
TP29
4106
4105
7622
HEF4052
7635
LF353
REXT1
REXT3
LEXT1
LEXT3
R-OUT
L-OUT
EXT2
7620
HEF4052
7630
LF353
TP19
9629
9658
LEXT2
TP22
TP17
TP21
TP18
TP20
TO SOUND AMPLIFIER
3680
TP9
7680
TDA8425
2684
2686
CONST. LEVEL
PSEUDO
TP8
TP11
7704
LM833
3722
3700
3720
TP10
CL16532027/011,FL-1

Fig. 4.1


TP8
6V
1V6
0,2ms/DIV
TP12
0V
1V6
0,2ms/DIV
TP17
0V
1V6
0,2ms/DIV
TP21
0V
1V6
0,2ms/DIV
TP9
6V
1V6
0,2ms/DIV
TP13
0V
1V6
0,2ms/DIV
TP18
0V
1V6
0,2ms/DIV
TP22
0V
1V6
0,2ms/DIV
TP10
0V
20mV
0,2ms/DIV
TP15
3V
0V7
0,2ms/DIV
TP19
0V
1V6
0,2ms/DIV
TP29
2V
0V3
TP11
10mV
20mV
0,2ms/DIV
TP16
3V
1V
0,2ms/DIV
TP20
0V
1V6
0,2ms/DIV

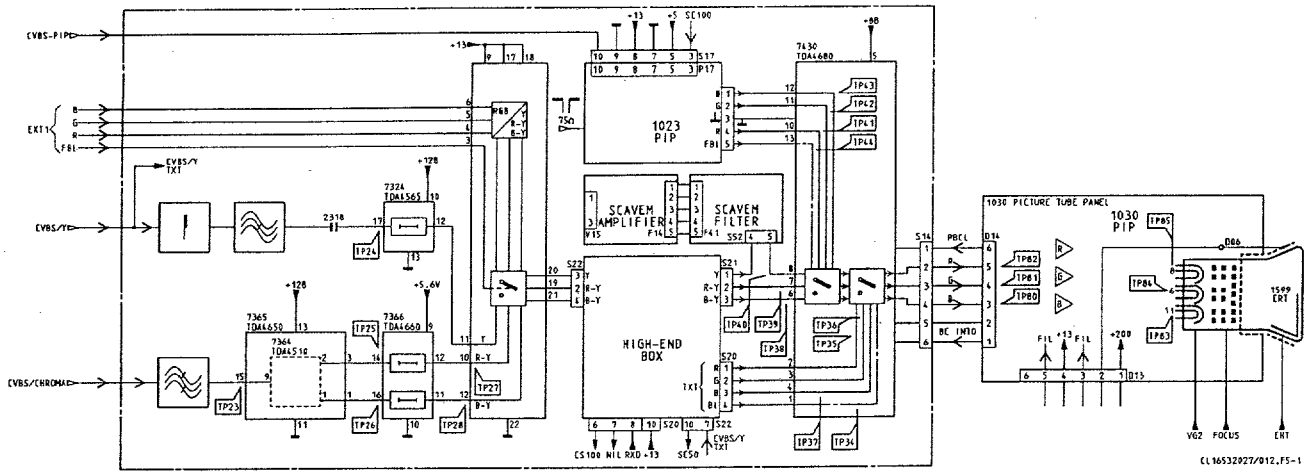
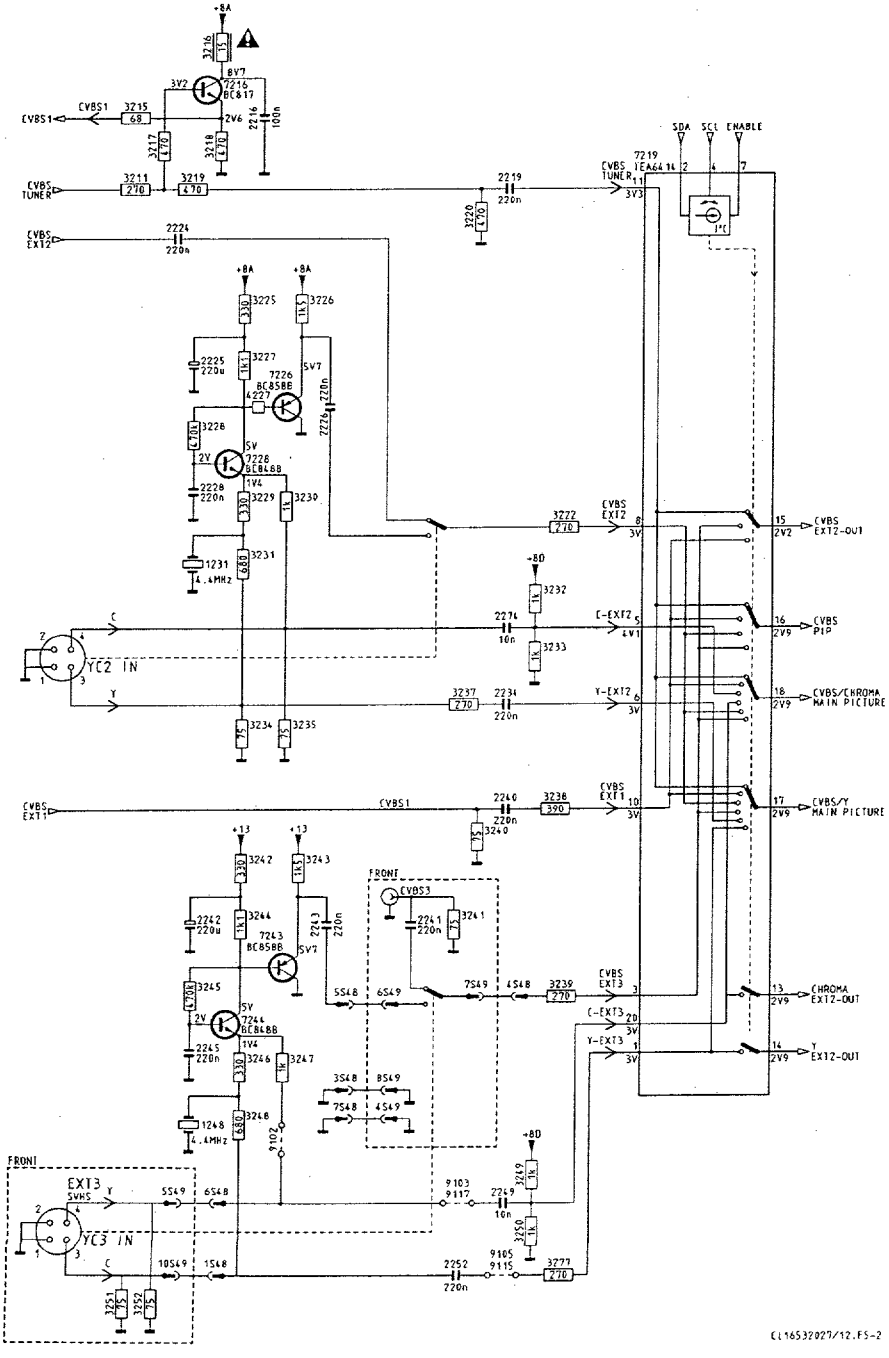


Fig. 5.1



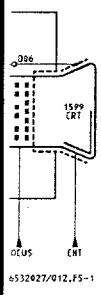
Content

Block

IC7364
= I
IC7365
= I

CTI = c
impr

Contents



Block diagram

IC7364 = TDA4510
= PAL
IC7365 = TDA4650
= PAL/SECAM/NTSC

CTI = colour transient
improvement

CHAPTER 5 THE VIDEO PATH

The CVBS/CHROMA signal coming from the video source selector is fed via an input filter to IC7364 (or IC7365), see fig 5.1.
The demodulator in the TDA4510/TDA4650 demodulates t signals and has the -(R-Y) and -(B-Y) signals as output. The colour difference signals are sent to IC7366 (TDA4660), th baseband delay line.
The -(R-Y) and -(B-Y) output signals from the delay lines are fed to IC7324 (TDA4565), the CTI-IC.The CVBS/Y signal coming from the video source selector is fed via a sharpnes circuit and a switchable chroma trap to a programmable del line incorporated in the CTI-IC.
The delayed Y signal and colour difference signals are finall fed to IC7430 (TDA4680), the video control IC, which converts the colour difference signals into RGB signals. The video control IC has also separate RGB inputs for RGB from EXT 1 or PIP and for TXT signals. Brightness, contrast and colour saturation control as well as cut-off stabilization also take place in the video control IC.

5.1 Source selection (Fig 5.2)

The video signal required for the main picture (chrominance and luminance), the external 2 output and the PIP picture is selected in input selection IC7219 (TEA6414).
Here the video signals may originate from:

- The front end
  The CVBS signal is supplied to pin 11 of IC7219 (TP30).
- Euroconnector 1
  The CVBS signal is supplied to pin 10 of IC7219.
  The CVBS status information (pin 8) of this euroconnector is fed to the microprocessor. The output of EXT-1 (pin 19) always receives the CVB signal from the front end (TP30).
- Euroconnector 2
  The CVBS signal is supplied from this euroconnect to pin 8 of IC7219.
  The output of EXT-2 (pin 19) receives an output signal that is selected by the selector switch (IC7219).
- The SVHS input
  Luminance is supplied to pin 6 of IC7219.
  Chrominance is supplied to pin 5 of IC7219.
  A CVBS signal is formed from the SVHS chrominance and luminance signals for the PIP module with TS7228 and TS7226.
- Ext-3 (The front CVBS connection)
  This signal is supplied to pin 3 of IC7219.

5.2 The luminance path

Sharpness circuit

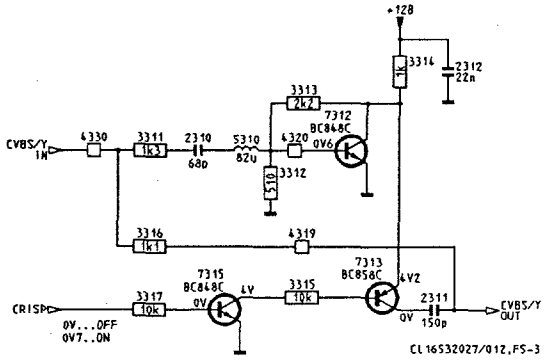


Fig. 5.3

The CVBS or Y signal coming from the video source selector is fed to the sharpness circuit. In the sharpness circuit the signal follows 2 paths, see fig 5.3.The first one is a direct path via R3316.
The second path goes via C2310, L5310 and TS7312. C2310 and L5310 form a band-pass filter tuned to approx 2 MHz. The 2 MHz component leaving this filter is amplified by TS7312.
If sharpness is switched on (crisp = high), TS7313 will conduct via TS7315 and the direct signal and the 2 MHz component will be added together.

Chroma trap

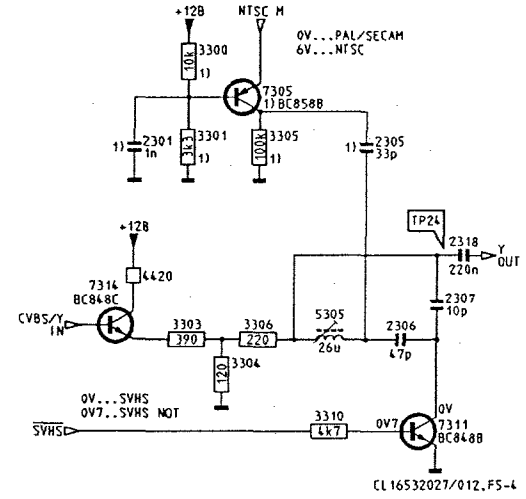
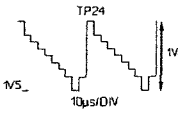


Fig. 5.4



The CVBS or Y signal coming from the sharpness circuit is buffered in TS7314 and the level is adjusted by R3303 and R3304.
At the output of this buffer is a switchable chroma trap, see fig 5.4. The function of this filter is to suppress the chroma signal in the CVBS/Y signal. There are four possible situations:

PAL/SECAM
During PAL/SECAM execution the SVHS switching signal coming from the microcomputer is high. Consequently, TS7311 is conducting.
The NTSC M switching signal coming from TDA4650 is low. This means that TS7305 is blocking current.
This results in a trap composed of L5305 and C2306 which is tuned to 4.43 MHz.

PAL/SECAM SVHS
With a PAL/SECAM SVHS signal, the SVHS switching signal will be low. TS7311 will block current in this situation. The result is no chroma trap.

NTSC M
In this case both TS7305 and TS7311 will conduct. This results in a parallel switching of C2305 and C2306. The chroma trap (which was tuned to 4.43 MHz during PAL/SECAM) will be detuned at 3.58 MHz.

NTSC M SVHS
TS7311 blocks current and TS7305 is conducting, resulting in a trap formed by L5305 and C2305. This trap is tuned to approx. 5.5 MHz.
There is no need for a chroma trap during SVHS signals.

Luminance delay in TDA4565

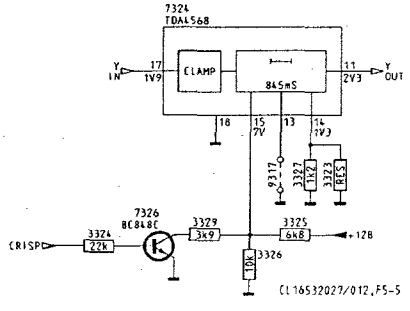


Fig. 5.5

The Y signal coming from the chroma trap is fed to pin 17 (TP24) of TDA4565, the input for the luminance delay line.
The delay of this delay line is adjusted by a DC voltage of 7.5V at pin 15.
If sharpness is switched on there will be less delay in the luminance line. Via TS7326 the voltage of pin 15 decreases to 0V and the delay will be adapted.

PAL chroma band-pass filter

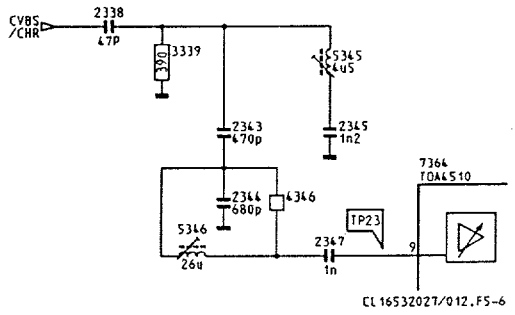


Fig. 5.6

Multi chroma band-pass filter

5.3. The chroma path

The CVBS/chroma signal is fed to a chroma band-pass filter.Two cases can be distinguished: PAL chroma band-pass filter in case of a PAL chroma decoder (TDA4510) and a Multi-standard chroma band-pass filter in case of a multi-standard chroma decoder (TDA4650).

C2338 and R3339 constitute a high-pass filter see fig 5.6. L5345 and C2345 form a suction circuit at 2.2 MHz. The parallel circuit L5346 and C2346 forms a band stop filter tuned to 5.5 MHz. All these circuits together form a band-pass filter tuned to 4.4 MHz.

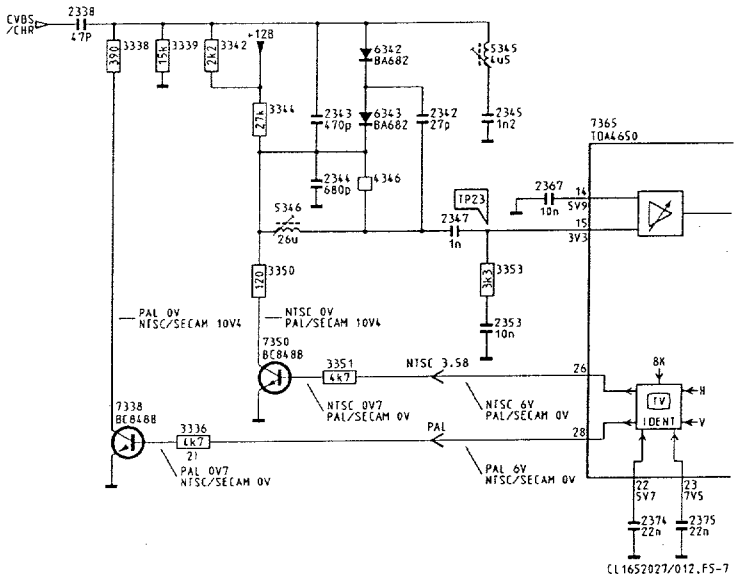


Fig. 5.7

PAL

Here, TS7338 is driven into conduction and TS7350 is cut off. C2338 and R3338 form a high-pass filter. L5345 and C2345 form a suction circuit at 2.2 MHz. The parallel circuit L5346 and C2346 forms a high-pass filter tuned to 5.5 MHz. The total once again results in a band-pass filter tuned to 4.4 MHz.

SECAM

Here, both TS7338 and TS7350 are cut off. The 2.2 MHz and 5.5 MHz band-pass filters result in an inverted bell-shape curve with its maximum at approx. 4.3 MHz.

NTSC 3.58

Here, only TS7350 is conducting. As a result, D6342 and D6343 are also conducting, causing C2342 to be in parallel with C2346 and L5346. C2343, which forms a voltage divider with C2344, is short-circuited. The band-stop filter formed by parallel circuit L5346, C2346 and C2342 is tuned to 4.5 MHz. The total results in a band-pass filter tuned to 3.6 MHz.

PAL chromadecoder

The PAL chroma signal is presented to pin 9 (TP23) of TDA4510 (fig 5.6). This signal is demodulated and decoded into baseband B-Y and R-Y signals, which are available at pins 2 and 1 (fig 5.1).

Multi chroma decoder

The multi-standard chroma signal (PAL, SECAM or NTSC 3.58) is presented to pin 15 (TP23) of TDA4650.
The systems are recognized by the colour burst or the identification signals (in case of SECAM) on the back porch of the CVBS signal.

The identification circuit in TDA4650 (Fig. 5.8) recognizes these signals and renders one of the 4 output pins high. In this way the chroma input filter is changed over.

Servicing hint:
by applying 12V to one of these four pins, the switches are put in the desired positions. This can be used to facilitate fault-finding. The identification circuit changes over the necessary circuits inside the IC.

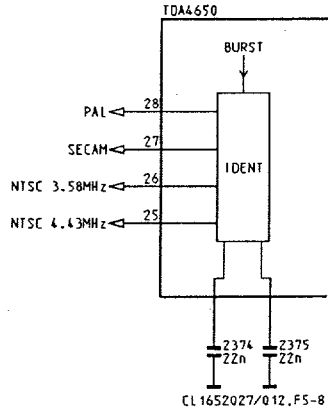


Fig. 5.8

The B-Y and R-Y signals coming from the colour decoder, see fig 5.9, are fed to the baseband delay lines in TDA4660 (IC7366). The direct signals and the ones delayed one line duration are added together.

The corrected B-Y and R-Y signals appear at pins 12 and 11 of TDA4660.

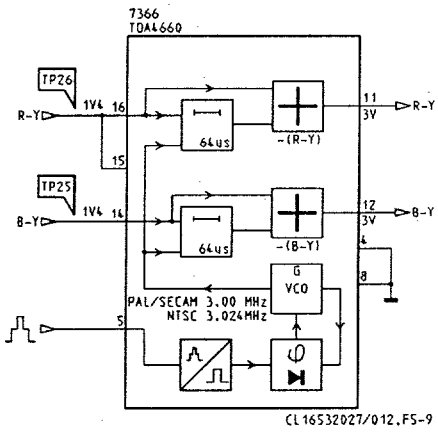
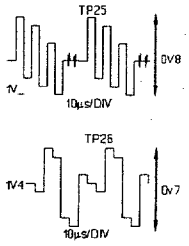


Fig. 5.9



5.4 The RGB matrix (and source selection)

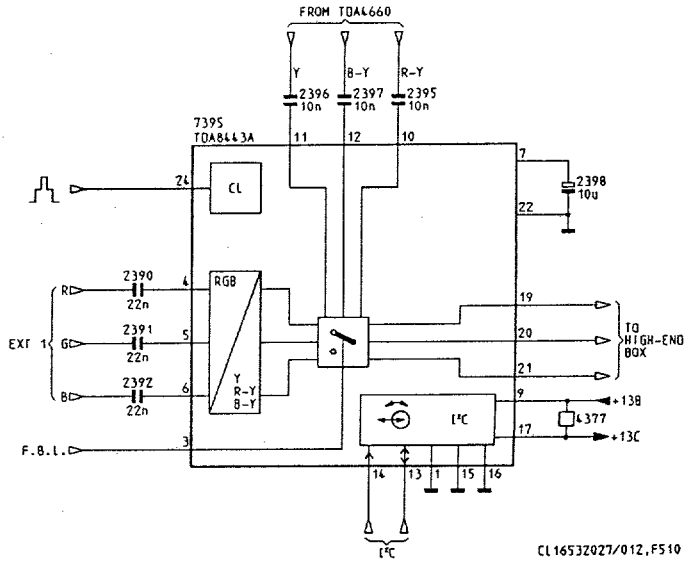


Fig. 5.10

In IC7395 the R,G,B signals coming from Euroconnector EXT 1 are converted into R-Y, B-Y and Y signals. Then, using the RGB status (pin 3) a choice is made between these signals formed from R,G,B and the signals coming from the chrominance and luminance processing.
The selected signals are supplied to the high-end box via pins 19, 20 and 21.

The principle of time compression

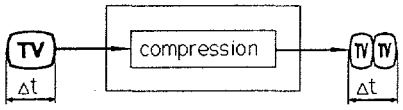


Fig. 5.11

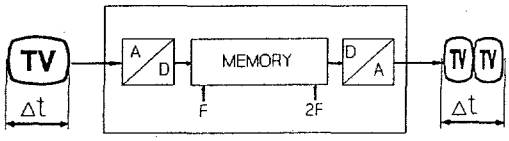


Fig. 5.12

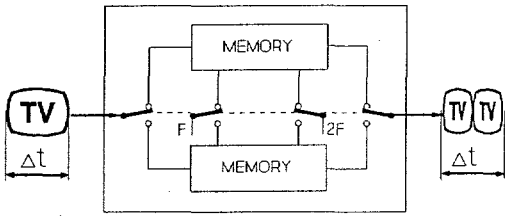


Fig. 5.13

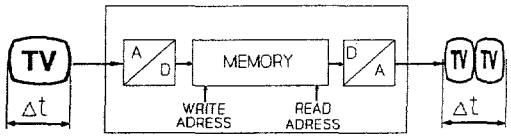


Fig. 5.14

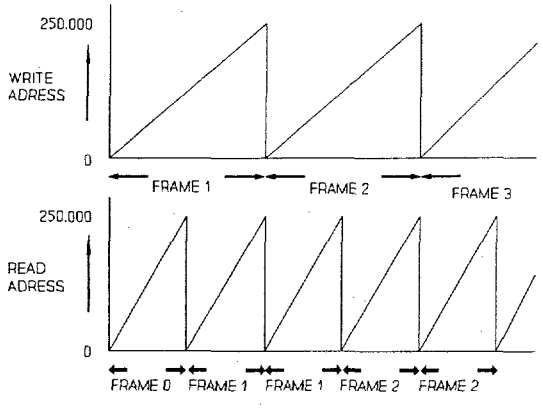


Fig. 5.15

5.5 The high-end box

As in a 100 Hz colour television receiver each picture must be written twice, in the same time span as a single picture with a 50 Hz receiver the video information must be doubled and compressed in time (fig. 5.11).

In practice this time compression is frequently carried out as follows (fig. 5.12).
The incoming video signal is digitised by an analogue-to-digital converter. Using a write clock signal with frequency F, the digitised picture information is then written to the memory.

Then with a read clock signal of frequency 2F the digitised picture information is read twice from the memory. As the reading out twice takes place twice as quickly, it takes just as long as writing once. The read-out signal is then made analogue again with a digital-to-analogue converter.

In order to obtain continuous time compression two memories are frequently used (fig. 5.13), where writing to memory I and reading from memory II (2x) is always alternated with reading from memory I (2x) and writing to memory II.
Signal compression in the high-end box.

Time compression in the 100 Hz conversion box of chassis FL1
is always carried out on a complete frame. As when using the previously described method two complete frame memories (total approximately 10 Mbit) are required in that case, in order to save memory use is made of another method in the FL1 conversion box (fig. 5.14).

Here one memory block is used which can contain a complete frame, where writing and reading can take place at the same time. Writing takes place here on a write address to be given and reading on a read address to be given.

The read and write addresses are controlled as shown in fig. 5.15. As shown in fig. 5.15, one frame is still being read out when the following is already written. Halfway through the writing of a frame the reading of that frame starts for the first time. Just before the following frame is written, the reading of the previous frame starts again.

For precise conversion of a complete frame each time the memory addressing signals must be coordinated precisely. This is done using the line and frame synchronisation signals. In order to reproduce picture signals compressed in time, the corresponding synchronisation signals must also be accelerated. As with these signals the phase and frequency are important, they are not generated with a memory but by software. Because the line and frame synchronisation signals are required for both memory addressing and synchronisation conversion, the frame and line synchronisation production and the read and write signal generation can be easily combined.

lock diagram

The total block diagram looks as follows.

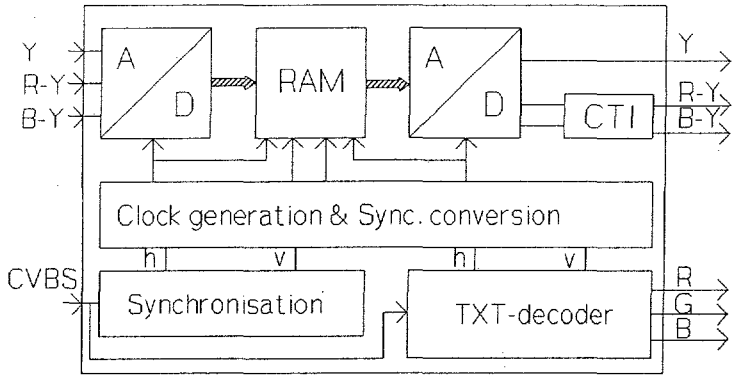


Fig. 5.16

The following parts can be distinguished here:

The synchronisation
IC7203 (TDA2579) supplies the synchronisation of the input signal of the high-end box for the operation (transmitter recognition and coincidence), the teletext decoder and the 100 Hz conversion control.

The digital video processing section
in which the incoming Y, R-Y and B-Y signals are digitised, converted into signals with a frame frequency of 100 Hz and than made analogue again. This is done using clock signals from the clock generation section.

The clock generation synchronisation conversion section
in which the clock signals for the digital video processing section are generated using the incoming frame and line synchronisation signals, and in which the 100 Hz/31250 Hz frame and line synchronisation signals are also produced.

The teletext decoder
in which the teletext information which is sent together with the transmitter signal is decoded and teletext pages are generated for reproduction on the screen.

The CTI (colour transient improvement)
with which the colour transitions are improved. Because these transitions are also affected by the doubling of the frame and line frequency, this improvement cannot be made on the 50 Hz signal side.

Synchronisation

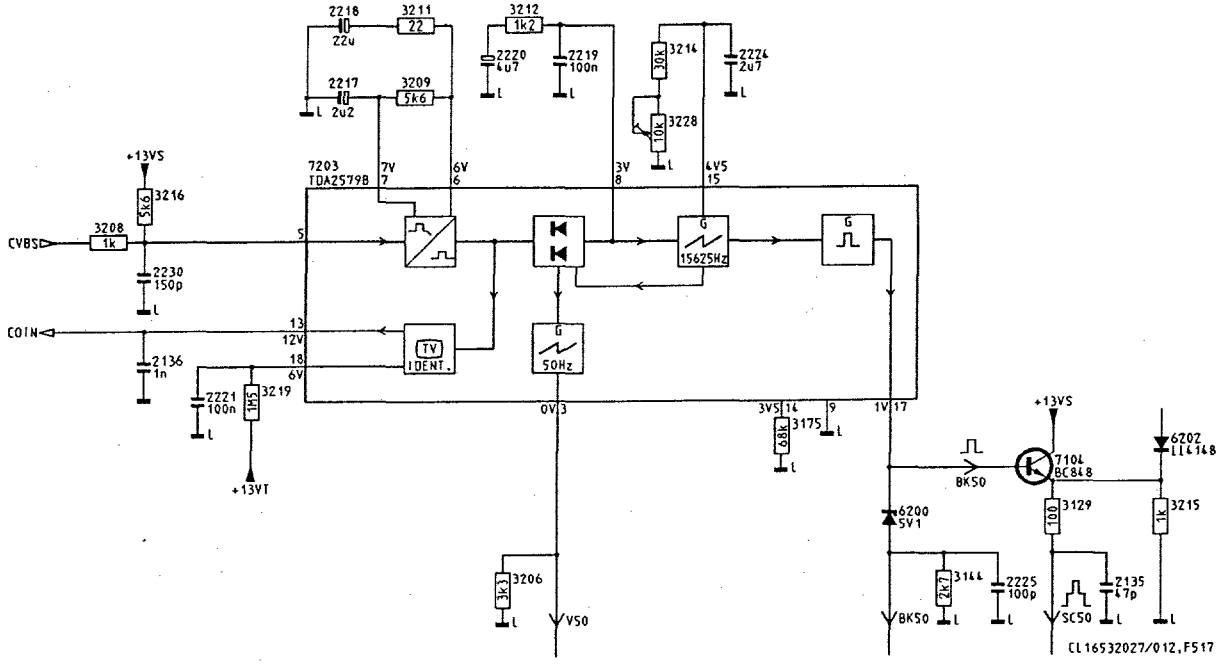


Fig. 5.17

Sync. separator

The CVBS signal goes to the sync. separator (A) via pin 5-IC7400. This detects the sync-top level and black level and stores them in C2217 and C2218, pin 6-IC7400 and pin 7-IC7400, respectively.

Time constants

The synchronisation can operate with 3 different control speeds depending on the quality and the size of the CVBS signal supplied at pin 5-IC7400. It is possible to measure which time constant is switched on at pin 18-IC7400.

Line oscillator

The horizontal oscillator (B) operates with the charging and discharging of C2224 at pin 15-IC7400. R3228 enables control of the charging and discharging time and thus the free-running oscillator frequency can be adjusted.
The free-running frequency can be adjusted by short circuiting the CVBS signal at pin 5 to earth and making the picture stable with R3228.
The burst-key pulse which is carried out via pin 17 is generated from the horizontal oscillator.

Vertical synchronisation

The vertical synchronisation (C) is derived from the horizontal synchronisation.
The vertical synchronisation signal is taken to the 100 Hz conversion control via pin 3.

Sandcastle generator

A sandcastle pulse is built up from the burst-key pulse at pin 17-IC7400 and the blanking pulse generated by the 100 Hz conversion control. This output signal has two levels:
1: 11V burst-key
2: 4.5V line blanking

This sandcastle pulse is taken to the small signal panel and is used by the chrominance decoder.

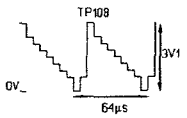
The teletext decoder

The teletext decoder consists of a video input processor (IC7200/SAA5235), a computer-controlled teletext IC (IC7201/SAA9042) and a RAM memory (Random Access Memory) (IC7202/41464). For a detailed description of computer- controlled teletext, see the CCT description published previously (4822 727 ....). The teletext decoder used here is different to the extent that the pages are generated with a 100 Hz frame frequency. Together with the corresponding fast blanking signal, the R,G,B signals produced are taken to the video controller on the small signal panel via pins 1 to 4 of connector H20.

The digital video processing

The signal path for the Y signal is described in this section. If the signal path for the R-Y and B-Y is different, this is also described.

The input circuit



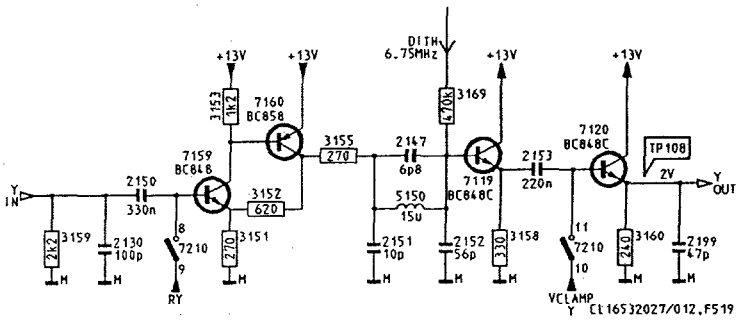


Fig. 5.18

The incoming Y signal via plug 3H22 is from the RGB converter TDA8443 on the small signal panel. The Y signal is first clamped with the burst-key pulse on a reference voltage using a switch in IC7210 and buffered with TS7159 and TS7160. The R-Y and B-Y signals are not clamped here.
Via a low-pass filter (formed by C2151, C2147, C2152 and L5150) and emitter followers TS7119 and TS7120, this signal goes to the analogue-to-digital converter (IC7213).
Via resistor R3169 a 6.75 MHz clock signal is added to the Y signal. The resistance value of R3169 is set so that the level of this signal is equal to half of the signal level of the least important bit used. This means that normally this signal will not be visible in the picture. However, in the case of a slow transition the signal becomes visible now and then, which results in an apparent improvement in the resolution.
The signal is clamped again after capacitor C2153.

The A/D converter

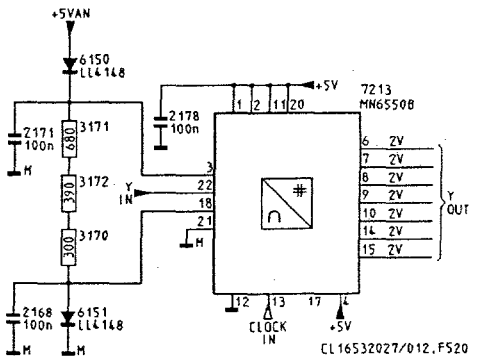


Fig. 5.19

The analogue-to-digital converter (ADC) receives the Y signal at pin 22 and a clock signal at pin 13. The clock frequency is 13.5 Mhz, which results in a maximum video bandwidth of 6.75 Mhz. The reference voltages of these ADCs are 4V3 (+5V - 0V7 (over D6150)) at pin 3 and 0.7V (over D6151) at pin 18.
The analogue-to-digital converter converts the input signal into a 7-bit code at pins 6,7,8,9,10,14 and 15.

R-Y and B-Y bit rate conversion

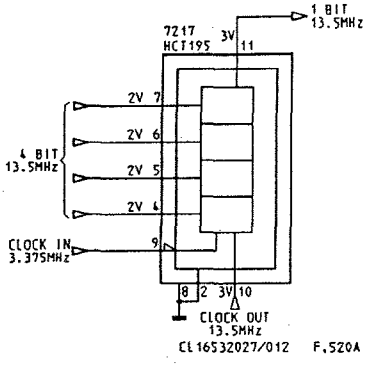


Fig. 5.20

The memories

The converted digital Y information is supplied to the memory. The converted digital R-Y and B-Y information does not go directly to the memory, but goes first to the shift registers IC7214 to IC7217. These signals do not in fact need the bandwidth of the A/D converter (6.75 MHz) (a bandwidth of 1.5 MHz is more than adequate). The R-Y and B-Y data are thus first reduced in bandwidth by a factor of 4. This is done by reading them in to the shift registers with a clock frequency of 3.375 MHz (CLK2) (for each 4 bits 3 are thrown away here).
The bits are then read out serially with a clock frequency of 13.5 MHz. Four parallel bits now remain of the 14 original parallel R-Y and B-Y bits.
These bits are now taken to the memory.

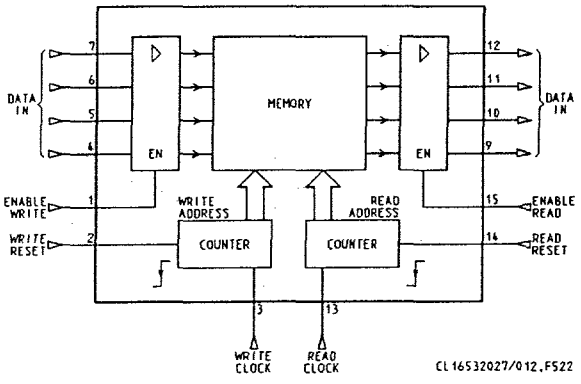


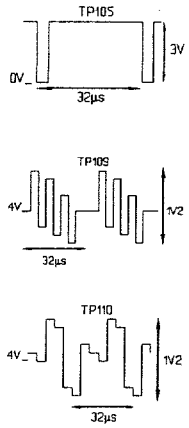
Fig. 5.21

The memory used is built up of 3 special video memories each of 1 Mbit (total 3 Mbit).
As the memory ICs can operate in parallel, they can all operate with the same clock signals. The memories are built up as follows (fig. 5.21).

There are 250,000 memory locations for 4 bits. The memory address written to is determined by the write address counter. This increases the write address by 1 for each clock pulse (starting with address 000000). If a reset pulse is given, the counter is blocked and the counter is set to zero on the down-sloping flank of this pulse, after which a new cycle will start. As the reset pulse is also linked with the write enable input, it is not possible to write during the reset pulse. The memory is read out in the same way, however the read and write address counters are given separate pulses. The write clock frequency is 13.5 MHz, and the read clock frequency is 27 MHz. The repetition frequency of the write reset pulse is 50 Hz and that of the read reset pulse 100 Hz. With a write clock frequency of 13.5 MHz, 18.5 ms of video information can be written to this memory. As one frame lasts 20 ms, information must be thrown away. This is done by not writing the invisible lines during the frame flyback.

The digitised picture information is read from the RAMs at pins 9 to 12. The pull-up resistors at the outputs ensure that the outputs do not stray during a read enable (during the reset pulse), but are defined high.

The D/A converters



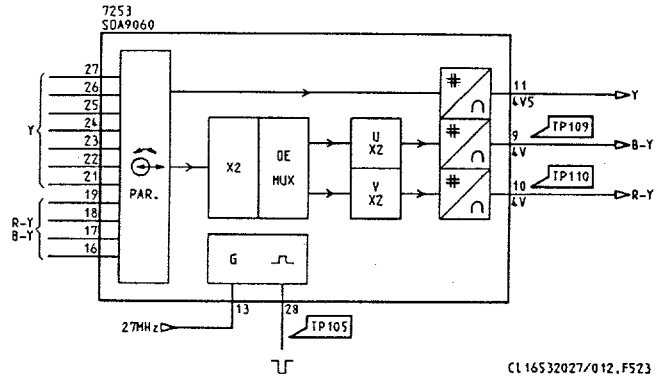


Fig. 5.22

The 100 Hz Y, R-Y and B-Y information is supplied to a digital-to-analogue converter (IC7253). The 4-bit R-Y/B-Y information is converted here to 7-bit R-Y and 7-bit B-Y, with a sample frequency of 27 MHz. Y, R-Y and B-Y then go to 3 A/D converters, after which they leave IC7253 again at pins 11, 9 and 10.
The read clock signal (27 MHz) comes in at pin 13 of the digital-to-analogue converter and this is used as a conversion clock. Pin 8 is the reference input. The reference is obtained from D6250.

CTI

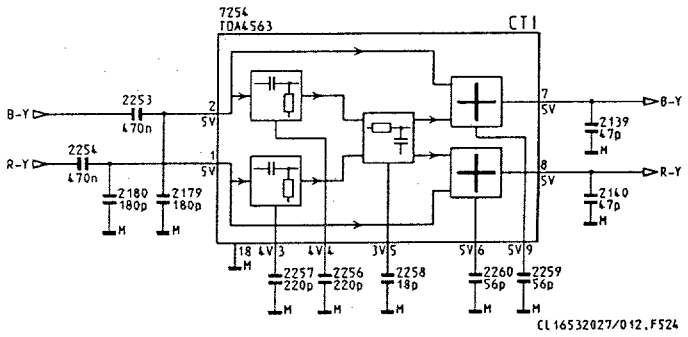


Fig. 5.23

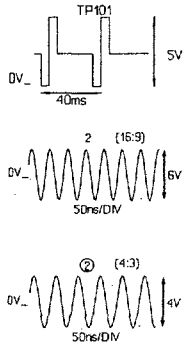
The Y-signal of the D/A converter first goes through a low-pass filter L5102/C2125.
R-Y and B-Y go to IC7254 for colour transient improvement. In the R-Y and B-Y signal path the steep signal flanks, colour transients thus, are made even steeper. At points where there are no steep flanks in the colour difference signals, colour surfaces for example, the input signals are passed on unchanged to the output.

The clock generator synchronisation converter

Microcomputer IC7204 (8051) and IC7205 (Programmable Signal Placer) together form the core of the clock generator and synchronisation conversion section. Using the connected electronics, the following subfunctions are available:
- The write clock generator
- The read clock generator
- The reset generation
- The synchronisation conversion
- The sandcastle generation
- The (non) interlace compensation
- The "watch dog" generator

These various functions are now discussed below.

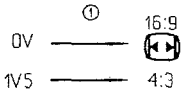
The 13.5 MHz write clock generator (Fig. 5.24)



If the control loop is working properly, the oscillator frequency must be exactly 13.5 MHz (when a standard TV signal is used). If this is the case, then in addition to a part of IC7205, a part of IC7204 also works and the communication between these ICs.

The write clock generator is built up around transistor T7116. Together with L5100 and C2111, this forms a free-running oscillator which is tuned to approximately 13.5 MHz. Via inverters in IC7206, the signal is supplied to pin 40 of IC7204. This is the input of a frequency divider. There is now a derived clock frequency at pins 41 to 45, or equal to the input clock divided by 2, 3, 4, 6 and 12. Of these the signal at pin 41 (6.75 MHz) divided by 2 is used in the input circuit. As this clock generator works independently of the other section of IC7507, these signals must always be present.
A derived frequency divided by 864 (= 15625 Hz) is supplied to a phase comparator (MC1 HI count). This compares this frequency with the burst-key information which comes in at pin 2. The phase information obtained from this comparison (DBK = digital burst-key) is carried out via pin 1 and is used to adjust the oscillator around transistor T7116 with varicap diode D6102 via R3119 and R3121.

4:3 compress mode (only for FL1.2)



If the unit is switched to 4:3 mode, the picture must be reduced horizontally. This is done by reducing the frequency of the read-in clock from 13.5 MHz to 10.125 MHz. If the reading out of the memory is also delayed slightly, a 4:3 picture will now appear in the centre of the screen.
The oscillation frequency is reduced as follows.
Pin 25/IC7204 is normally high, TS7102 conducts and diodes D6106 and D6107 conduct. Coil L5110 is now bypassed by D6107 and will not affect the oscillation circuit. The oscillation frequency is now 13.5 MHz.
In 4:3 mode pin 25 will be low and TS7102, D6106 and D6107 do not conduct. Coil L5110 now affects the oscillation frequency and will shift this to 10.125 MHz. In order to achieve this, the control circuit must also be modified. The oscillation frequency is thus now divided by IC7205 by 648 (= 15625 Hz) before this is compared with the 50 Hz burstkey.

Movie expand

In the movie-expand mode a 4:3 picture is reproduced horizontally as a 16:9 picture and in addition expanded vertically. This vertical expansion does not take place in the high-end box, but in the vertical deflection circuit (Section 6 The read-in clock in the high-end box in this case is at 13.5 MHz.

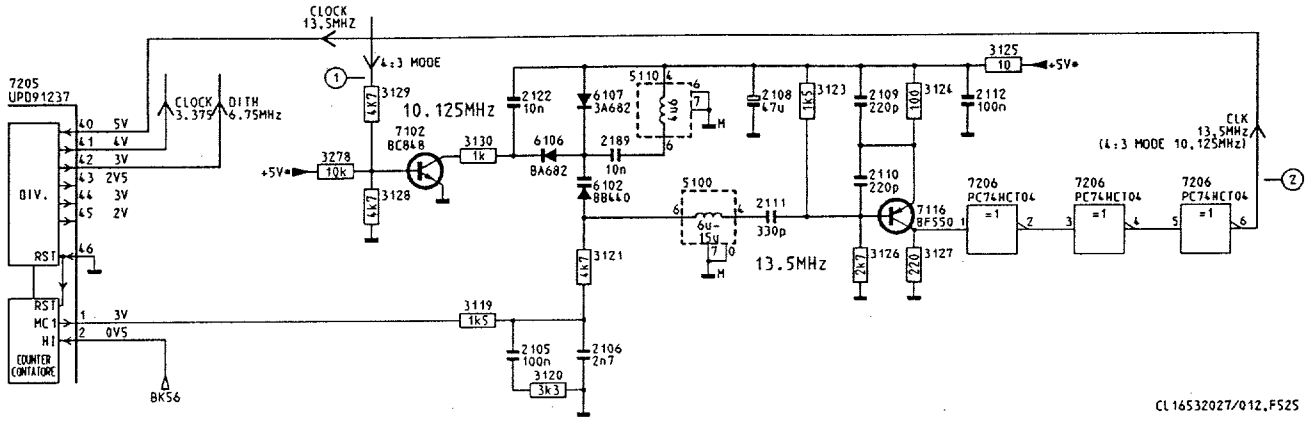


Fig. 5.24

The 27 MHz read clock generator.

The read clock generator is built up around transistor 7117. The read clock generator is also a free-running oscillator which is set to approximately 27 MHz with L5101/C2117. Via inverters in IC7207, this oscillator signal is supplied to a frequency divider in IC7205 (pin 33). This divider works independently of the other part of IC7507, and supplies the clock frequency divided by 12, 6, 4, 3 or 2 at pins 28 to 32 A signal divided by 1728 (15625 Hz) is supplied to a phase comparator (MC2 HU count) which compares this signal with the burst-key signal.

The phase information obtained from this comparison comes at pin 26 from the IC, passes the low-pass filter R3140/R3138/C2188 and via R3137 adjusts with varicap diode D6103 the oscillation frequency of the oscillator built up around TS7117.

If the control is working properly, the oscillation frequency must be exactly 27 MHz (when a standard TV signal is used

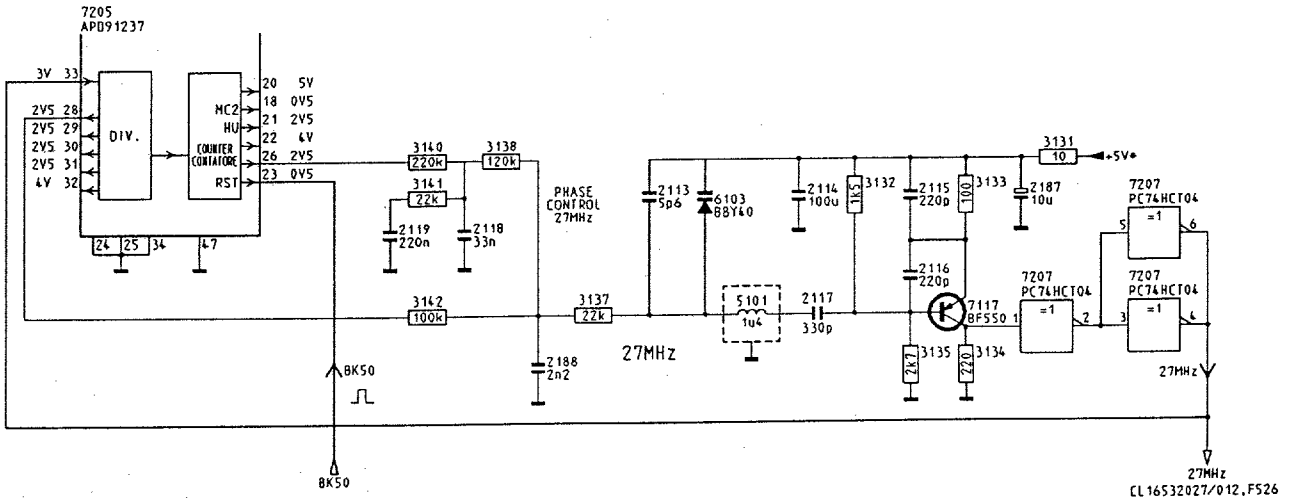


Fig. 5.25

Reset generation

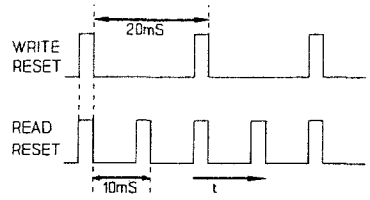


Fig. 5.26

From the incoming 50 Hz frame synchronisation signal, the incoming burst-key signal (BK) and the generated write clock signal, a write reset signal (WR) is generated (pin 37), which ensures that one complete frame is always written to the memory. From the generated 100 Hz frame synchronisation signal, the generated line sync. signal and the generated read clock signal, a read reset signal (RR) is generated (pin 36), which ensures that one complete frame is always read twice from the memory. These signals must be generated accurately so that the correct frame is always written or read. The signals look as follows (fig. 5.26).

Synchronisation conversion

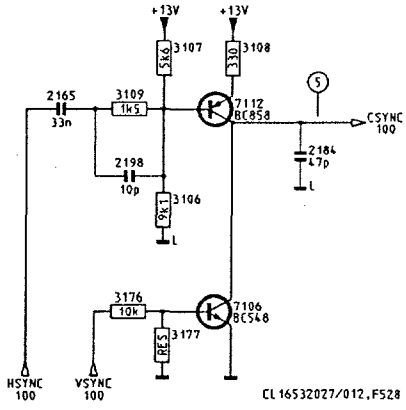


Fig. 5.27

Horizontal (31250 Hz) and vertical (100 Hz) synchronisation pulses (coming from pin 18 and pin 19, respectively) are generated by IC7204 and IC7205. Via TS7112 and TS7106, they are added together and supplied as a composite synchronisation signal to the small signal panel via connector 6H20.

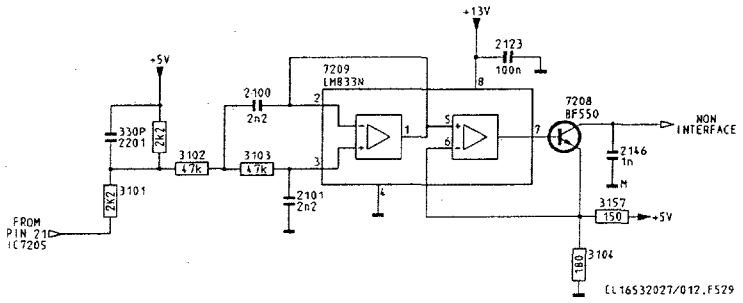


Fig. 5.28

Interlacing compensation

In order to reproduce teletext information non-interlaced, a NIL signal is generated at pin 21/IC7205; this is amplified by IC7209 and sent to the vertical deflection via TS7108 and 7H20.

The "watch dog" generator

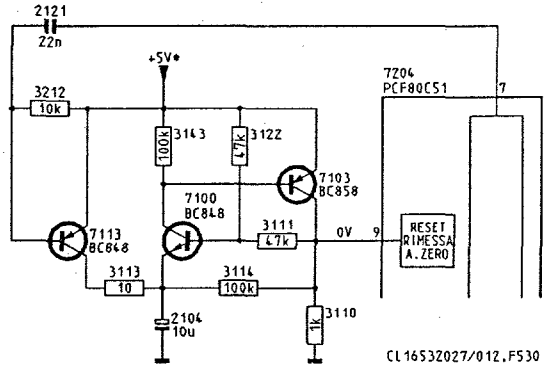


Fig. 5.29

The circuit around transistors T7113, T7100 and T7103 is a "watch dog" generator. Its function is to check that microcomputer IC7204 is working. If it is not, the circuit will give reset pulses in order to start up the microcomputer. This circuit works as follows:
TS7100 would normally be opened via R3122, which would then make TS7103 conduct, after which a reset pulse is given to pin 9/IC7204.
During the programme of IC7204, however, pin 7 is made alternately high and low. The pulses generated in this way are passed to TS7113 by C2121. These will now conduct periodically, which charges C2104. Consequently, the emitter of TS7100 has a higher voltage and will therefore not start to conduct. However, as soon as the programme of IC7204 stops, the pulse train at pin 7 will disappear and a reset pulse will be generated at pin 9.

5.6 SCAVEM (FL1.2)

R-Y, B-Y and Y for the main signal and R,G and B of teletext come from the high-end box. Together with the PIP signal, these are supplied to the video controller. The Y signal coming from the high-end box also goes to the SCAVEM circuit.

Introduction

A picture tube has a fairly large capacity relatively speaking (in electrical terms it can be regarded as a capacitor). Consequently, white to black transitions are reproduced less quickly than black to white transitions. In fact, in the first case the picture tube capacity must be discharged. With a 4:3 receiver this is not a problem, however with a 16:9 receiver the picture is stretched horizontally, which means that these transitions can be seen more clearly. SCAVEM is added in order to obtain even black/white and white/black transitions.

SCAVEM

SCAVEM stands for **SCA**n **VE**locity **M**odulation. Here the velocity of the electron beam is adjusted horizontally over the screen depending on the picture content. The velocity of the beam is increased with black/white transitions (they are thus less sharp) and reduced with white/black transitions (they are made sharper).
In FL1.2 SCAVEM is built up on 2 panels: the SCAVEM filter panel and the SCAVEM amplifier panel. In addition, there is an extra coil attached to the neck of the tube which carries out the actual modulation.

SCAVEM filter

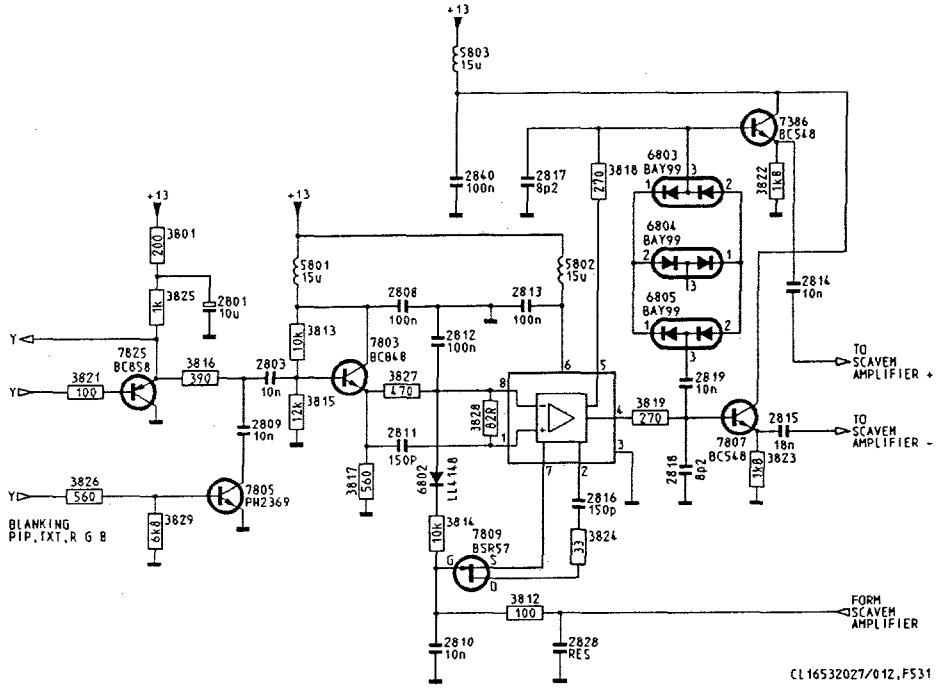
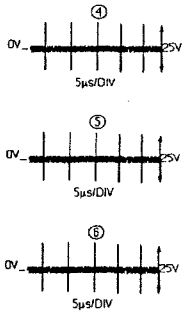


Fig. 5.30

The incoming Y signal is buffered and amplified with TS7801 and TS7802. The signal then goes through a low-pass filter with a cut-off frequency of 12 MHz.

Transistor TS7805 is supplied with the blanking signals of teletext and PIP. Here the Y signal is suppressed during the reproduction of these signals because no modulation can take place on this.
The signal is buffered again and then goes to IC7804. IC7804(NE592) is a symmetric video amplifier. Its output signal is a symmetric signal: the two signals are thus identical, but in opposite phase.
A three-times differentiator is built up around this amplifier. The first differentiator consists of the input circuit R3827, C2811 and C2812, the second of the feedback R3824, C2816 and the first of the output filters R3819, R3818, C2818 and C2817. The high frequencies in the video signal (and thus the sharp transitions) are amplified by these differentiators. TS7809 normally conducts, however if the SCAVEM amplifier becomes overloaded, it will stop conducting, which means that the amplification and with it the signal level decrease. The diode bridge D6803, D6804 and D6805 limits the signal amplitude to 1 V4. Transistors TS7806 and TS7807 buffer the symmetric signal, after which it goes to the SCAVEM amplifier panel.

SCAVEM amplifier



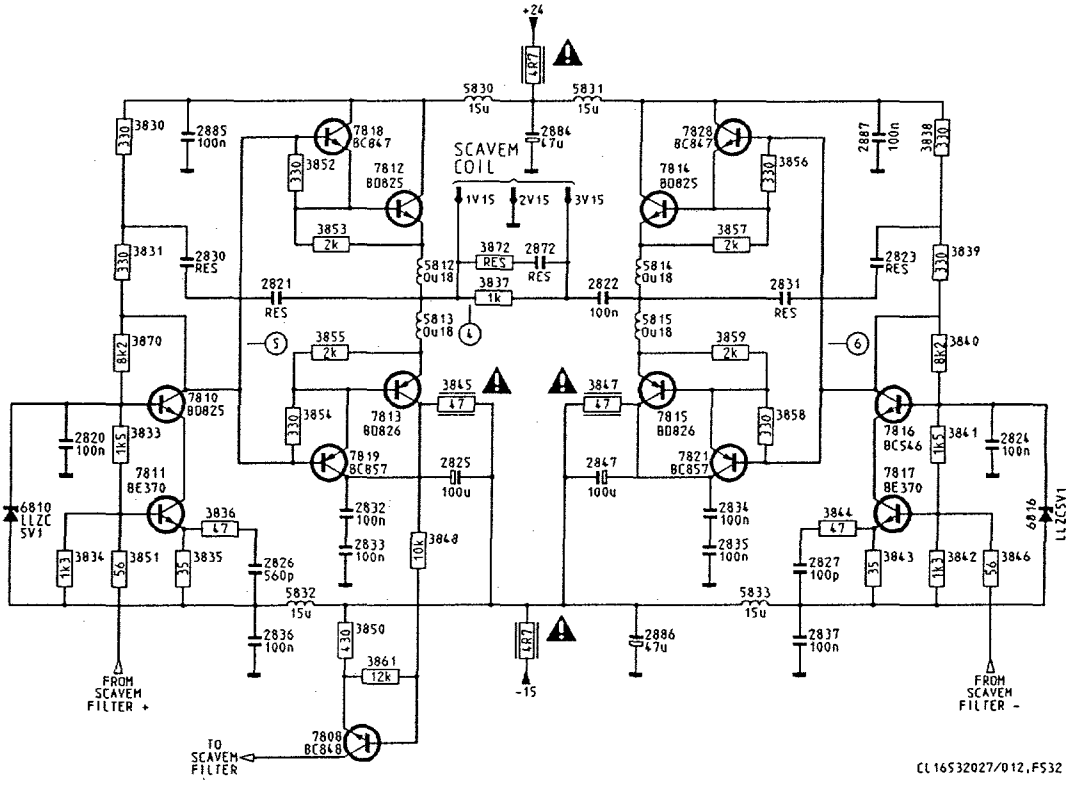


Fig. 5.31

There are two identical amplifiers on the SCAVEM amplifier panel. These consist of a voltage amplifier around TS7810 and TS7811 (TS7816 and TS7817) and a current amplifier around TS7812 and TS7813 (TS7814 and TS7815). The two amplifiers together control the SCAVEM coil. The current through the coil is measured over C2832 and C2833. If it is too high, TS7809 will start to conduct, which adjusts back the amplification on the filter panel.

5.7 Video controller (TDA4680)

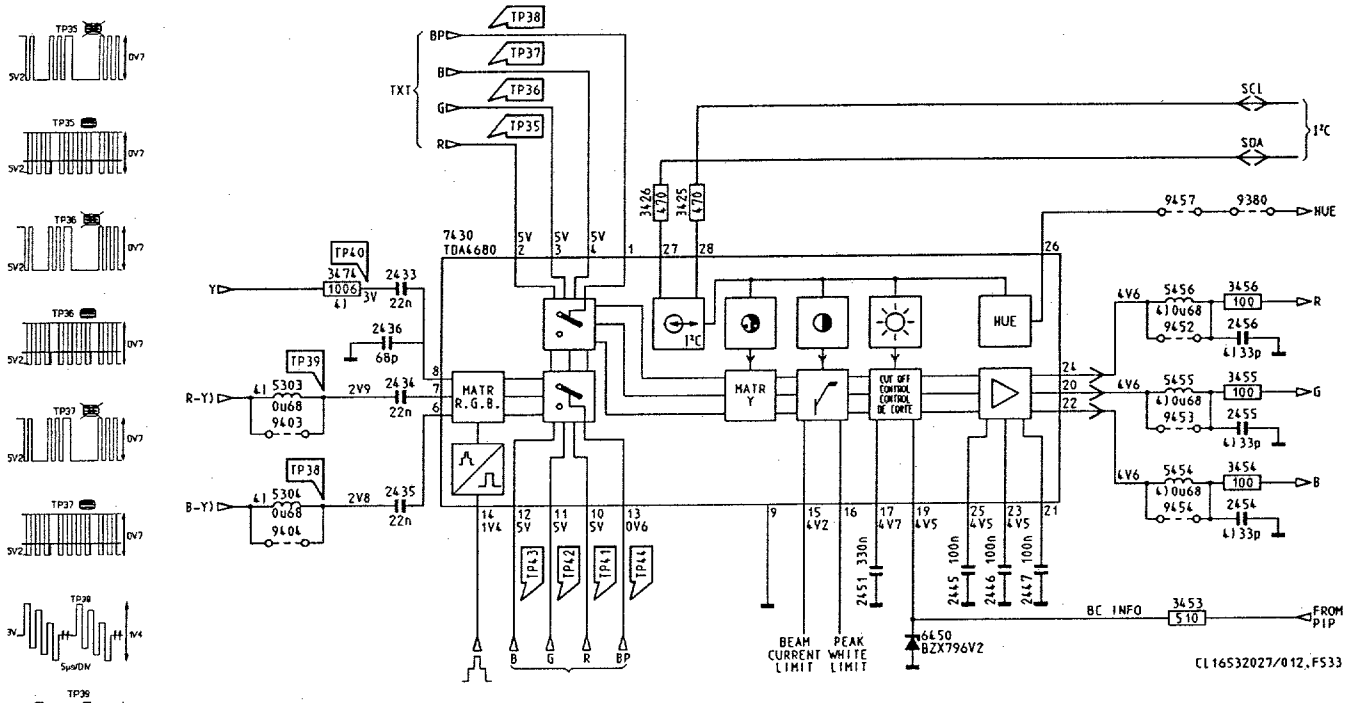


Fig. 5.32

The video control IC receives 3 input signals:

a. Y (TP40), -(R-Y) (TP39) and -(B-Y) (TP38) signals supplied by the High-end box.

b. R(TP41), G(TP42) and B(TP43) signals + RGB blanking supplied by the PIP module if present.

c. R(TP35), G(TP36) and B(TP37) signals + TXT blanking supplied by the teletext decoder.

With all these signals colour saturation, brightness and contrast can be controlled. In addition, a beam-current limiter and a cut-off stabilizer are present. The output signals are RGB signals which drive the RGB output amplifiers on the picture tube PC board.

If the voltage at pin 13 of TDA4680 is low, the Y, (R-Y) and (B-Y) signals are passed on to the control amplifiers. A high voltage at pin 13 switches the RGB signals coming from EXT 1 or PIP through to the control amplifiers.
A 2nd switch is controlled with the TXT blanking and switches the TXT signals through if pin 1 of TDA4680 is high.
Transistor 7410 enables a PIP to be written in teletext mode.

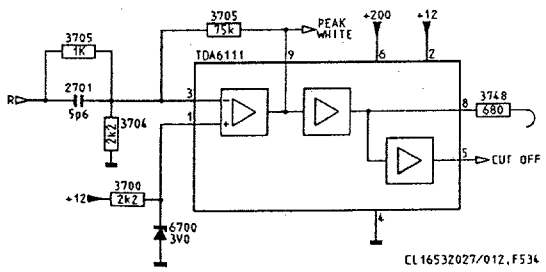


Fig. 5.33

5.8 RGB amplifiers (TDA6100)

The heart of the RGB output amplifiers is an integrated power amplifier, the TDA6100. For each colour one IC is used. The circuits for the three colours are identical.

Peak beam-current limitation

The peak beam-current information is measured limitation via diodes 6701, 6702 and 6703. If the voltage at one of the amplifiers drops below 40V (high beam current), TS7704 will start conducting, causing TS7450 and TS7451 to start conducting also. Consequently, the voltage at pin 16 of TDA4680 decreases and the peak white limiter becomes active. If the voltage on one of the amplifiers drops below approx. 20 V (very high beam current), zener diode 6707 will start conducting also, thus driving TS7704 fully into saturation. The peak white limiter then is driven to full power.

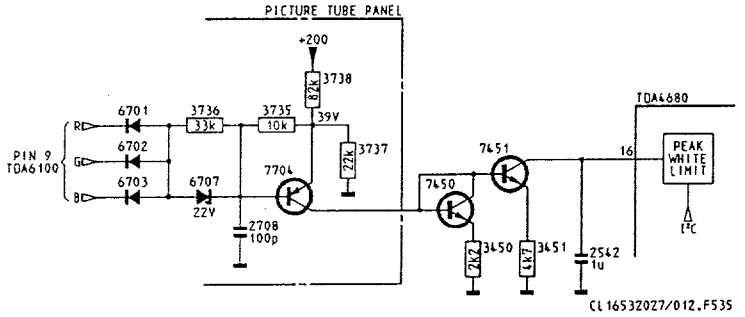


Fig. 5.34

Stabilization of cut-off points

During frame flyback a number of pulses are generated enabling the TDA4680 to set the cut-off points of the picture tube. The pulses are measured with R3710, R3719, R3753 and R3453 at pin 19 of TDA4680.

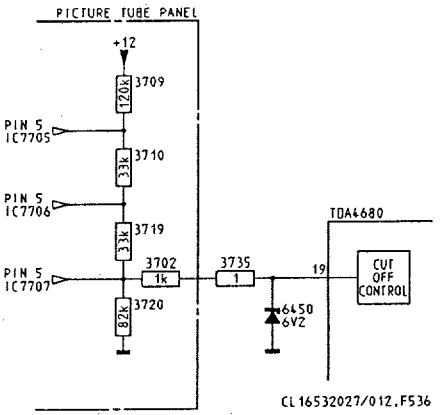


Fig. 5.35

6 Synchronisation and deflection

Contents

Block diagram (fig. 6.1)

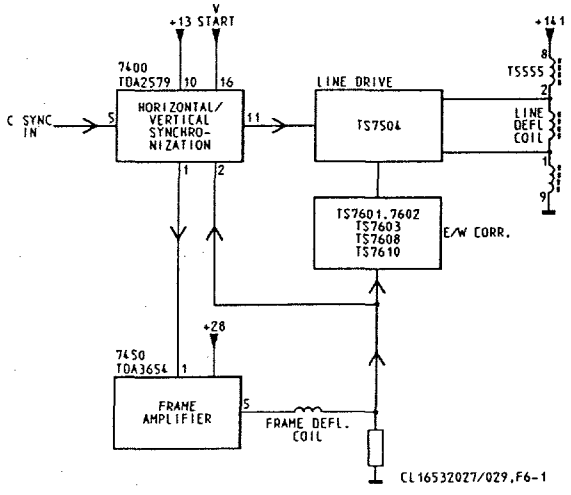


Fig. 6.1

The whole line and frame synchronisation takes place in IC7400 (TDA2579). The frame output amplifier is built up around IC7450 (TDA3654). The line output stage is built up around T5555 and is controlled via TS7501 and TS7504. The line output stage is powered from the main SOPS (+ 141), while the frame output stage is powered from the line output stage (+ 28).

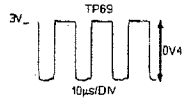
6.1 Synchronisation

IC7400 (TDA2579) (Fig. 6.2)

Starting up

IC7400 is started up in two phases.
After the set is switched on, the V-start supply voltage (chapter 7) only starts the horizontal oscillator (via pin 16-IC7400). After that the +13 supply voltage powers the other internal circuits via pin 10-IC7400. As a result, the line output stage will start up gradually after switch-on.

Sync. separator



The sync signal arrives at the sync separator via pin 5-IC7400. The sync separator detects the sync peak level and the black level and stores them in C2402 and C2403, pin 6-IC7400 and pin 7-IC7400 respectively.

Time constants

The synchronisation can work with 3 different control speeds depending on the quality and the size of the sync signal supplied to pin 5-IC7400 (TP69).It is possible to determine which time constant is switched on by taking a measurement at pin 18-IC7400.

Pin 5	Pin 18	time contant
no signal	< 1V2	small
signal	± 6V25	normal
good signal	± 10V	large

Line oscillator

The horizontal oscillator works on the principle of the charging and discharging of C2406 at pin 15-IC7400. R3406 makes the charge and discharge time controllable and thus the oscillator frequency adjustable.The free-running frequency can be set by short-circuiting the CVBS signal on pin 5 to earth and setting the picture stable with R3406.

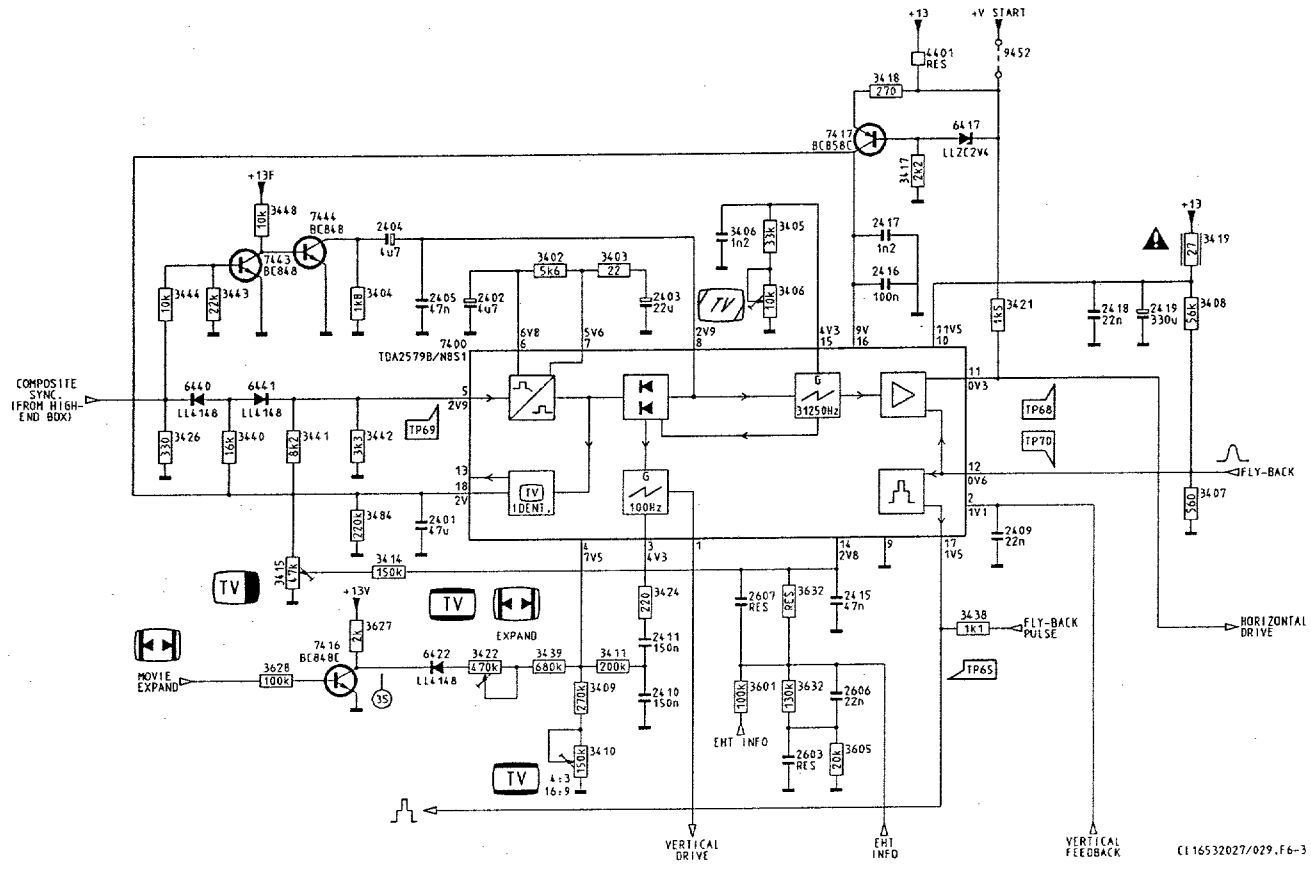
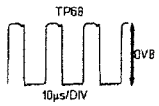


Fig. 6.2

ne output



The oscillator signal of the horizontal oscillator goes via the line pulse phase comparator to the output pin 11-IC7400 for control of the line output stage.
By varying the control voltage for the phase detector with R3415 (pin 14-IC7400), the moment of the flyback can be adjusted.
In this way the picture can be centred horizontally with R3415. However, because this control affects the linearity, the second control is added in the deflection circuit. Together with these two controllers, the horizontal centring can be adjusted and the linearity remains good.

ıase discriminator

The line output stage forms a flyback pulse, which is sent via pin 12-IC7400 to the phase discriminator. The latter uses this pulse to adjust the phase of the outgoing line pulses.

Vertical

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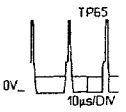


Burn-in

Field bla

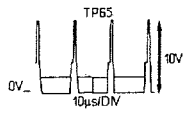
Vertical synchronisation

In this way, first R3410 (in 16:9 mode) and then R3422 (in expand mode) should be adjusted.

The vertical synchronisation is obtained from the horizontal synchronisation.With the components between pin 4 and pin 3-IC7400 the shape of the saw-tooth control voltage is determined for the frame output stage.

The picture height can be set using potentiometers R3410 and R3422. R3410 is used for the setting in normal 16:9 and 4:3 operation. In film format (movie expand) operation D6422 starts to conduct and the picture height can be set using R3422.

Sandcastle generator



The sandcastle pulse is at pin 17-IC7400. This output signal has three levels:
1: 11V burst-key
2: 4.5V line blanking
3: 2.5V frame-blanking

Burn-in protection

If the voltage fed back from the frame deflection (pin 2-IC7400) on this is greater than 1.9V or less than 0.5V, the sandcastle generator will increase the output (pin 17-IC7400) to a minimum of 2.5V.(Field blanking)

Field blanking

The raster blanking for PIP is generated by the high-end box. For the video controller the sandcastle is used for this. With film format (movie-expand) reproduction in FL1.2, however, writing would be both at the top and at the bottom in the picture tube. Thus in movie-expand mode an extra raster blanking is generated by the high-end box (VBl. 16:9), which is added to the sandcastle via IC7800.

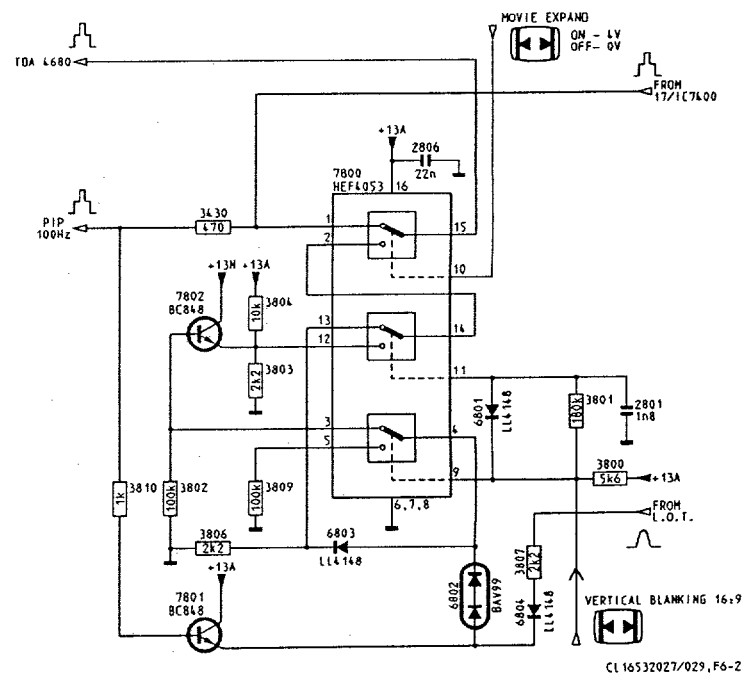
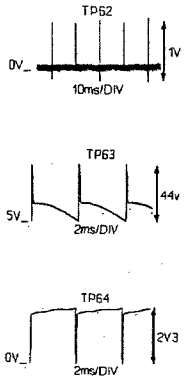


Fig. 6.3

6.2 The frame output stage (fig. 6.4)



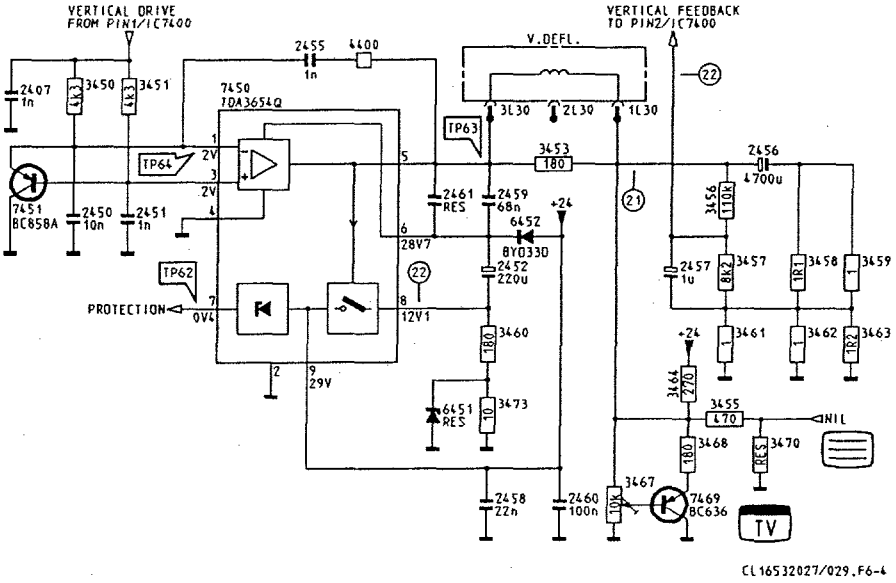


Fig. 6.4

The frame deflection is built up around two IC's:
-IC7400 (TDA2579) which contains the frame oscillator and the differential amplifier.
-IC7450 (TDA3654) the frame output amplifier.
Because the deflection coil forms a self-induction which resists any current change, the current through the deflection will not follow the shape of the connected voltage.
The current is therefore converted into a voltage over R3461/R3462/R3463 and returned via R3457/R3474/C2457 to pin 2-IC7400. There the shape of the voltage is compared with the shape of the control voltage at pin 3-IC7400.

Flyback generator

The frame output amplifier IC7450 is powered via pin 6 from the +28 supply voltage. This voltage is too low for a fast flyback. Therefore a flyback generator has been mounted around C2452. This generator is charged to 22 V during scan and to ± 50V during flyback. TS7451 takes care of a fast discharge of C2450 and thus for a steep side during frame flyback.

Picture height

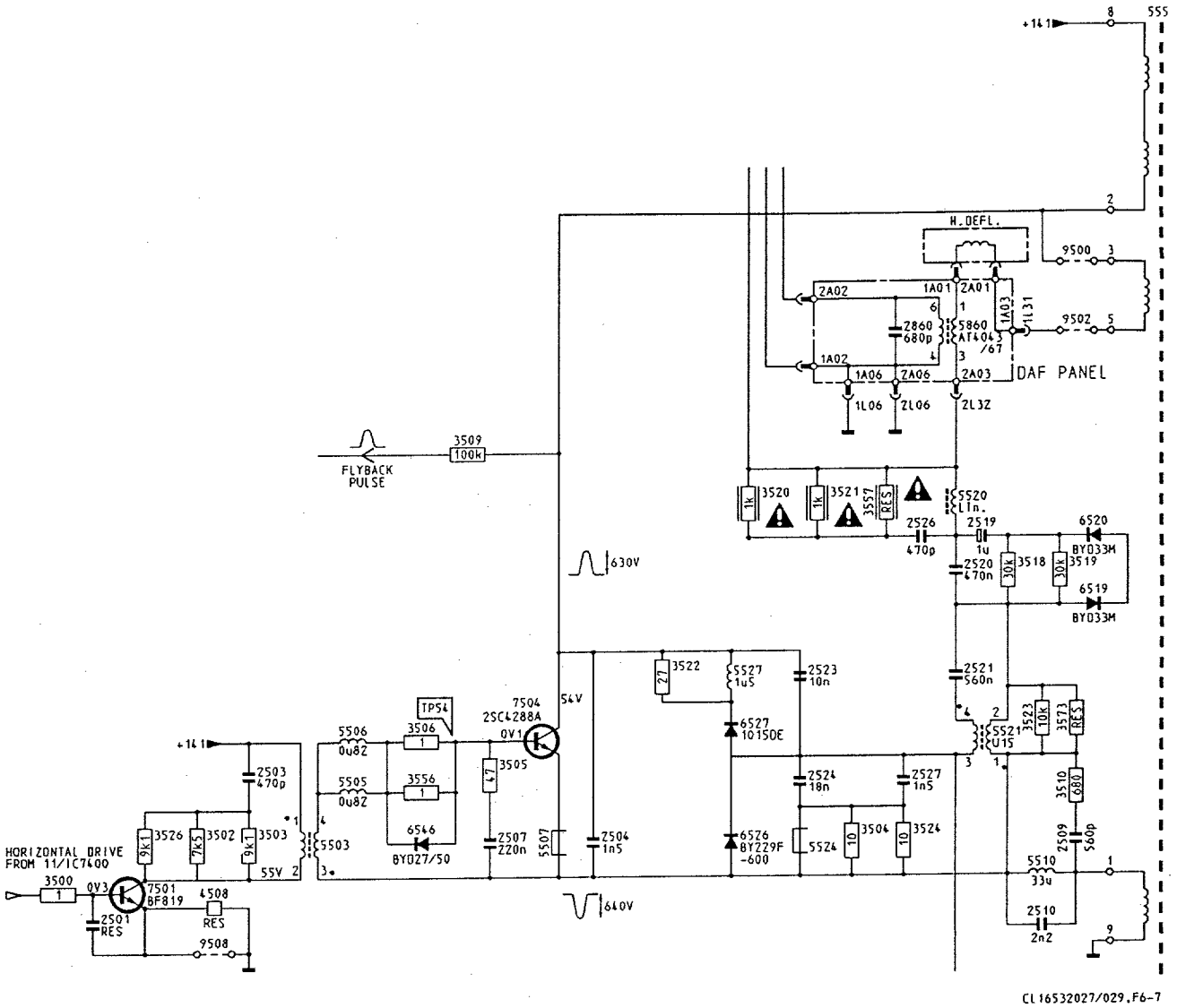
The picture height can be influenced by sending an extra direct current through resistors R3461/R3462/R3463, which measure the saw-tooth shaped current through the deflection coil and feed it back to pin 2-IC7400. This direct current is adjustable with R3467.
The picture height can be set with R3467.

Protection

If, because of a defect in the frame deflection, the voltage at pin 8-IC7450 drops below 1.5V, pin 7-IC7450 (TP62) will increase its voltage from 0.4V to 4.5V. This voltage will switch off the SOPS supply.
TS7480 prevents the protection from being activated erroneously during switching-on.
The voltage +5 from the line transformer at the moment of start-up will in fact not be present immediately, which causes TS7480 to conduct.

. 6.4)

6.3 The line output stage



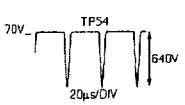


Fig. 6.5

The line pulses originating from pin 11 of synchronisation IC7400 are passed on via TS7501 and T5503 to switching transistor 7504 (Fig 6.5). The deflection circuit consists of line deflection coil 5627, switching transistor TS7504, flyback capacitor 2504 and capacitor 2520.

The power for the line output circuit is applied symmetricall via turns 8-2 and 1-9. This has the advantage that not one but two flyback pulses are formed, which are half the size and opposite to each other. Consequently, the amount of L interference dissipated is reduced. The control signal is not affected by this because it is applied via an electrolytic separation (T5503).

The flyback generator is consists of D6522, D6525 and T5521.

Corrections

The following correcting circuits have been incorporated in series with the deflection coil:

S-correction

The value of C2520 has been chosen such that the voltage across the deflection coil varies to keep the speed of the electron beam across the screen practically constant.

Horizon

Linearity

Coil 5520 is a premagnetized coil taking care that the voltage across the deflection coil does not progress exponentially during scan.

Other corrections

-The circuit consisting of S5510 and R3510 prevents the line transformer from decaying.

-The circuit consisting of C2519, R3518, R3519 and D6519, which is mounted parallel across C2520, is intended to prevent the decaying as a result of sharp white transitions.

East-West correction

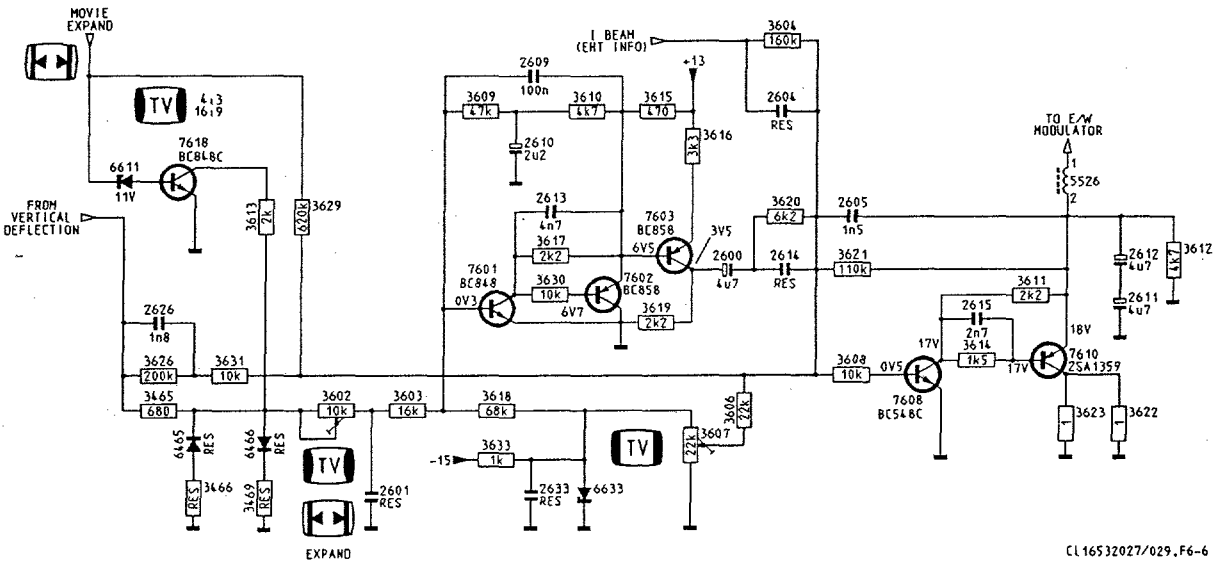


Fig. 6.6

For the East-West demodulator the flyback circuit has been divided into two parts. Both circuits are tuned to the same frequency (so they have the same flyback time). It is the intention that the supply voltage across the deflection circuit is modulated with a frame frequency, parabolic voltage.
This voltage is made from the vertical saw-tooth voltage by a double integrator (Fig 6.6) that is built up around TS7601, TS7602 and TS7603. In movie-expand mode the amount of East/West correction can be set with R3602. In normal 16:9 or 4:3 mode TS7618 starts to conduct and the correction is modified by R3629.
To prevent the picture width from varying along with the beam current, the east-west modulator is also supplied with the beam current information.
Potentiometer 3607 varies the DC-adjustment and thus the picture width.

Output

Horizontal shift

To shift the picture horizontally, a positive or negative current can be sent through the deflection coil with the aid of the circuit in Fig. 6.7.

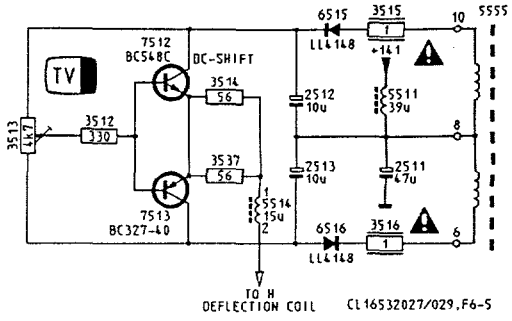


Fig. 6.7

Output voltages

The line output transformer delivers the following voltages:
- EHT, Focus and VG2
- Beam current information (EHT info)
- Heater voltage for the picture tube
- The +5, +28, -10 (-Vn) and +200 supply voltages.

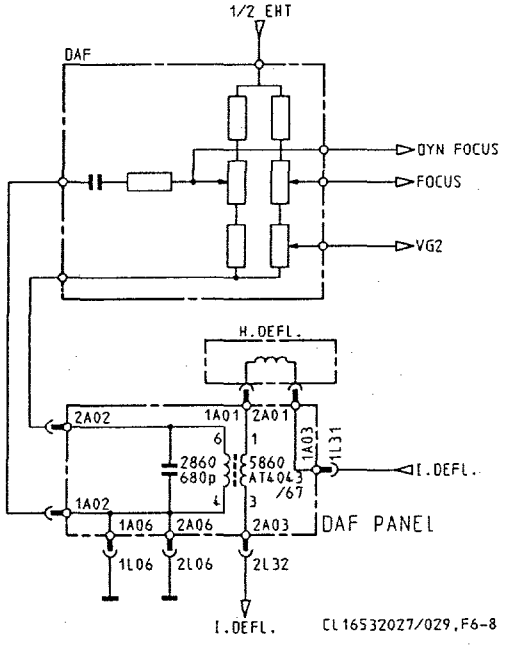


Fig. 6.8

6.4 DAF (Dynamic Astigmatic Focus)

Because of the large width of a FL1.2 television receiver, the distance from the electron gun in the tube to the sides of the screen is much greater than to the centre. Thus, the picture will normally not be in focus over the whole picture width. The Dynamic Astigmatic Focus unit has been added to solve this problem. The primary winding of transformer T5860 on the DAF panel is in series with the horizontal deflection coil. A sawtooth line frequency voltage now forms on the secondary winding. Together with C2860, the secondary winding forms a double integrator which converts this sawtooth voltage into a parabolic voltage. This is taken to the Focus/VG2 splitter.
The Focus/VG2 splitter is powered by the half high voltage. The VG2 and the focusing voltage are obtained from this. The focusing voltage is now modulated with the line frequency parabolic voltage formed on the DAF panel. Consequently, the focusing voltage will be different at the sides of the picture, and thus the picture is focused over the whole width.

7 Power supply

Contents

The FL1.0 sets are equipped with 2 supply circuits, namely a main supply and an auxiliary supply (stand-by supply).

7.1 The main supply

This supply is of the SOPS type (Fig. 7.1). A characteristic feature of the FL1.0 main supply is that the entire driver circuit (with the exception of the stand-by and protection parts) is located on a separate SOPS control PC board. This power supply delivers the +141, +16 and -16 (for the sound output stage) and the +13 supply voltages.

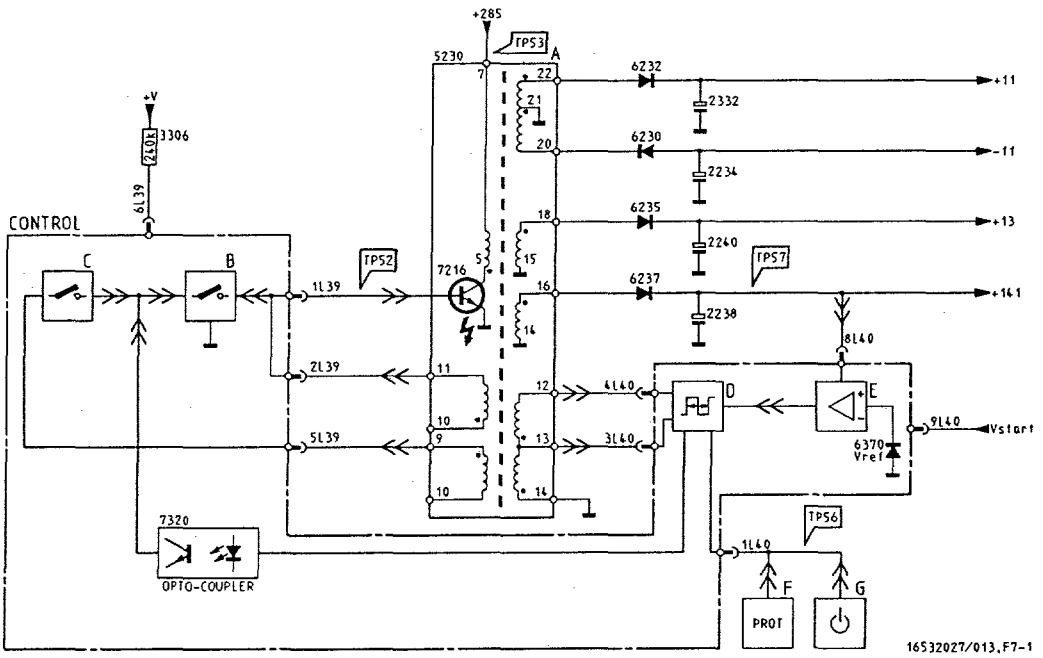
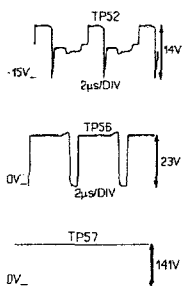


Fig. 7.1

Working



The mains voltage is rectified on the primary side (TP53). The power supply is started up via resistor R3306. The rectified voltage is fed to switching transistor 7216, which is driven by the circuit on the control PCB (TP52).
The control PCB accommodates both the primary and the secondary part of the control circuit. The stand-by circuit (G) and the protective circuit (F) are not located on the control PCB.
The primary control circuit, consisting of the switch-off circuit (B) and the blocking circuit (C), is driven by the secondary part (via an optocoupler) and by turns 9-10-11.
The secondary part contains a pulse width modulator (D), which is driven by turns 12-13-14 and by a voltage comparator (E). The latter adjusts the pulse width modulator with 141-volt voltage that is presented via pin 8L40.

Stand-by

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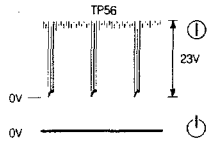


+11

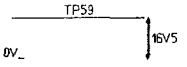
-11

+13

+141

Vstart

+ 13 Volt



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The power supply can be turned off via pin 1L40 (TP56). This takes place if the voltage at this pin drops below +/- 1 Volt (fig. 7.2).
In stand-by mode the control microcomputer generates a low level at the base of TS7385. Via TS7384 pin 1 of connector L40 is now connected to 0 V.
The main supply is now completely turned off and all output voltages are 0 Volts.

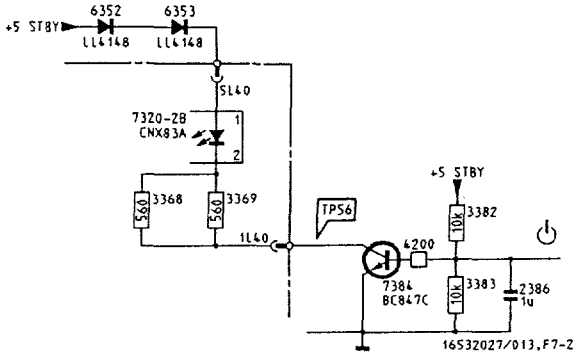


Fig. 7.2

Starting-up

The power supply can be adjusted back via pin 9L40; if the voltage at this pin is lower than 7 volts, the output voltages of the SOPS will be low, but the SOPS stays operational. For a good start-up of the line output stage when the set is switched on, first the auxiliary supply and then the main supply should be started. Therefore the +V start supply voltage of the auxiliary supply is fed to pin 9L40 of the control PCB. As long as this voltage is not available, the output voltages of the main supply stay low.

Most current for the +13 volts is supplied by resistor R3241 (Fig. 7.3).

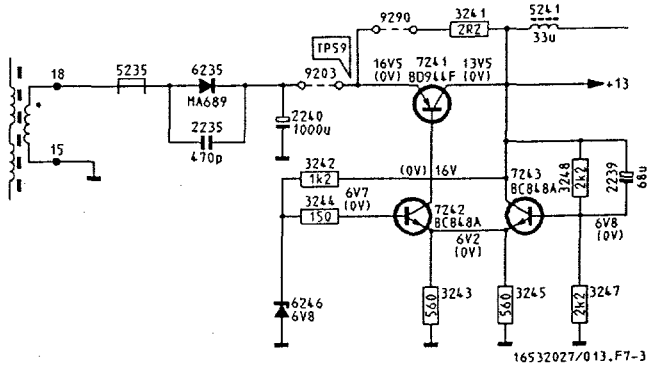
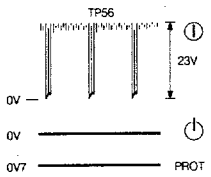
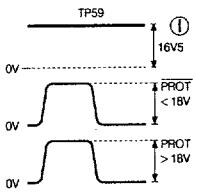


Fig. 7.3

However, its dimensions are such that during normal operation the output voltage is slightly less than 13 volts. Therefore an extra current is carried via TS7241, which brings the voltage at the required value of 13V. TS7241 is driven by the differential amplifier that is built around TS7242 and TS7243. D6246 delivers the necessary reference voltage.

Protection





The FL1.0 chassis is equipped with a number of protective circuits. If one of these circuits detects a fault, the main power supply will be switched off.
The protection is driven via the thyristor function that is built up around TS7380 and TS7381 (Fig. 7.4), and is activated by a pulse generated by one of the protective circuits.

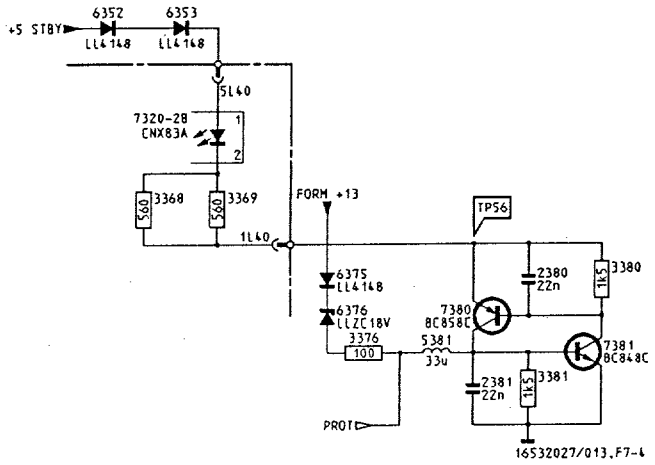


Fig. 7.4

If the protection is activated, pin 1L40 (TP56) will be kept low (0,7 volt) so that the main supply is switched off. The thyristor function will keep the power supply switched off, even when the fault is eliminated.

The following circuits are equipped with a protection:

Main SOPS

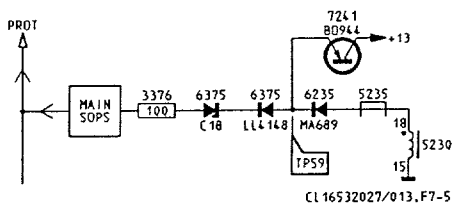
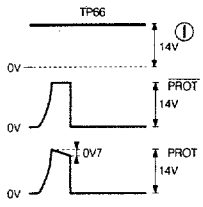


Fig. 7.5

In order to detect a possible overvoltage of the main SOPS the +13 output voltage is checked.
If the output voltage at the cathode of D6235 exceeds +19 volts, zener diode D6376 will start to conduct and activate the protection circuit.



EW circuit

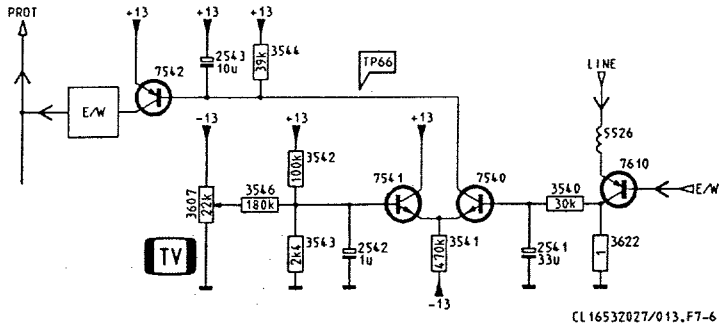
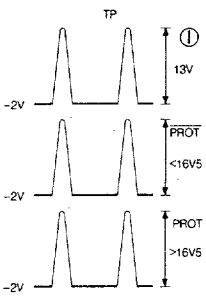


Fig. 7.6

Transistors 7540 and 7541 form a differential amplifier. The base of TS7541 can be set with R3607 (picture width control), whereas the base of TS7540 is driven by the collector of TS7610.
If a fault causes the voltage on the collector of TS7610 to become too high, TS7540 will start to conduct, thus activating the protection circuit via TS7542.

L.O.T.



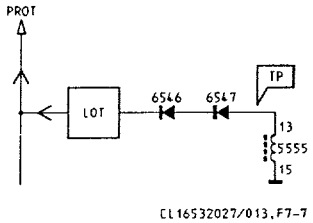


Fig. 7.7

The amplitude of the flyback pulse will increase if the flyback pulse becomes shorter, e.g. because of a fault in the line output stage.
The protection circuit will thus be activated via D6547 and D6546.

Beam current

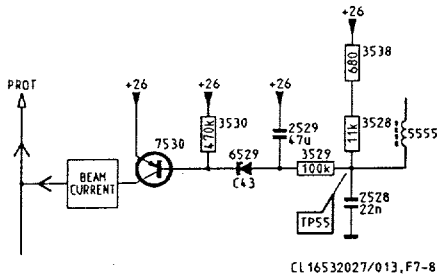
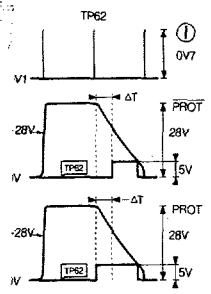


Fig. 7.8

If the beam current becomes too high, the voltage across C2528 will drop, thus causing D6529 to zener and the protection circuit to be activated via TS7530.



Frame deflection

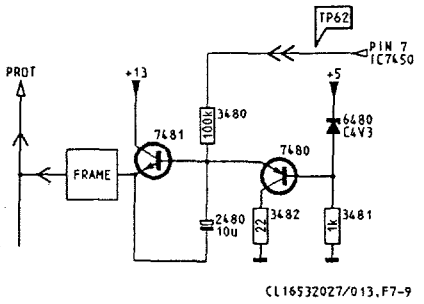


Fig. 7.9

At normal operation of the frame output stage pin 7-IC7450 is low, so that TS7481 blocks current.
If the frame deflection drops out, 7-IC7450 will go high, so that TS7481 starts to conduct and the protection is switched on.
At switch-off of the set, 7-IC7450 goes high. If the set is switched on and off very quickly, C2480 cannot discharge fast enough so that the protection becomes effective.
To avoid this, TS7480 has been added.
At switch-off, the +5 supply voltage drops out quickly, so that TS7480 starts to conduct and C2480 is discharged via this transistor.

Sound output stage

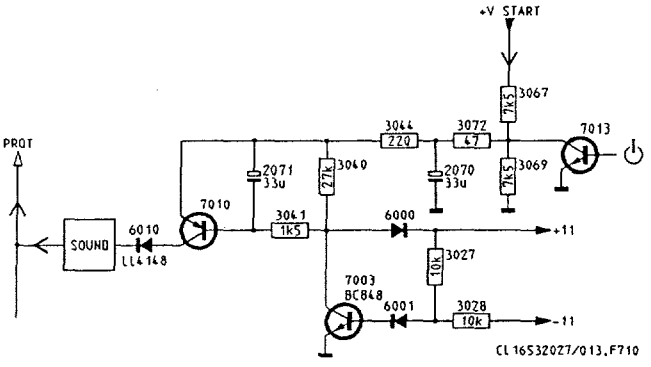
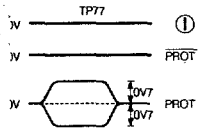


Fig. 7.10

Voltage division of the +16 and -16 results in a voltage of 0V at the junction of R3029 and R3007.
If the voltage at this junction exceeds 3,3V (D6002) + 0,6V (D6001) + 0,6V (be-TS7003) = 4,5V, TS7003 will start to conduct and the protection circuit will become effective via TS7010 and D6010.
If the voltage at the junction is less than -1.2V, TS7010 will also start to conduct.
If the +16 and the -16 are short-circuited with each other, TS7010 will be driven into conduction via D6000.
If the unit is set to standby, TS7013 will start to conduct, which means that no protection can be activated.

If, moreover, the average voltage supplied to one of the loudspeakers is not 0V, TS7003 or TS7004 will also be driven into conduction.



Fault detection

By fixing a measuring pin to a test point in one of the protected circuits, and then switching on the set, it can be checked whether that circuit activated the protective circuit.

7.2 The auxiliary supply (micro SOPS)

This power supply remains active when the set is in stand-by mode.

Block diagram

Primary
- blocking oscillator A
- switch-off circuit B
- switch-off accelerator F

Secondary
- variable load C
- voltage stabiliser D
- switch-on pulse generator E

The auxiliary supply is built up of 6 blocks:(Fig. 7.11)

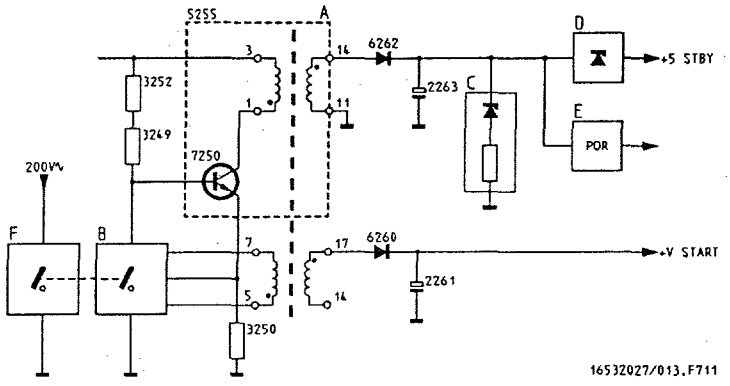
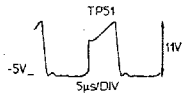


Fig. 7.11

Primary

Blocking oscillator
Transistor TS7250 receives it base voltage via R3252 and R3249 and starts conducting.
A linearly increasing current then starts flowing through winding 3-1 of T5255, TS7250 and R3250.



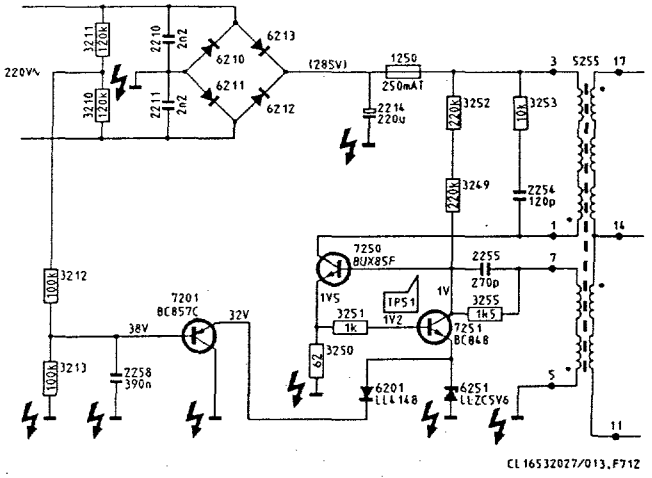


Fig. 7.12

Switch-off circuit

If the current increases, the voltage across R3250 increases as well. If this voltage exceeds the emitter voltage of TS7251, TS7251 will start conducting and TS7250 will be switched off. As the emitter voltage of TS7251 has been set at 5.6 V by D6251, the voltage across R3250 at that moment will be 6.2 Volts and the current approx. 90 mA. The polarity of the magnetic field in the transformer then is reversed and the voltage across winding 5-7 becomes negative. Transistor TS7250 is kept out of conduction via R3255/C2254 until all energy on the secondary side has been dissipated. Capacitor C2254 now constitutes an oscillator circuit with winding 3-1, so that an oscillation is formed. The polarity of the voltage across winding 7-5 is reversed via the magnetic coupling, thus causing a current to be delivered to the base of TS7250. This transistor starts conducting and the cycle above is repeated.

Switching off

The mains AC voltage is fed via R3210, R3211 and R3212 to the base of TS7201. If the mains voltage drops out (at switch-off), TS7201 will start conducting immediately and the voltage across zener diode D6251 will decrease. Consequently, the output voltages of the micro SOPS will decrease at once.

Secondary

On the secondary side 2 voltages are supplied:

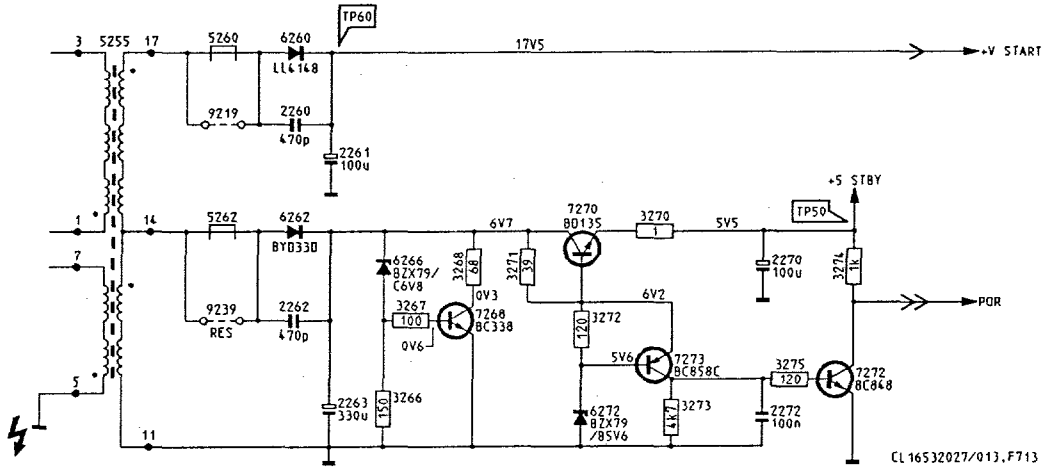
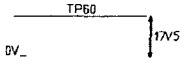


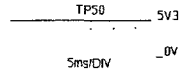
Fig. 7.13

+ Vstart



At pin 17 the Vstart voltage is supplied via D6260 across C2261. This voltage is used to activate the synchronisation IC and to let the main power supply know that the micro SOPS has been started up and that now the main SOPS may be started up as well.

+ 5 Stand-by



At pin 14 a voltage is supplied via D6262 across C2263 from which the +5-volt stand-by voltage is formed.
The +5-volt standby voltage is stabilised in 2 different ways.

Variable load

If the voltage across C2263 exceeds 6.9 volts, zener diode D6266 and TS7268 start conducting.
The power supply, then, is loaded extra by R3268, so that the voltage decreases more quickly.

Stabilisation

Series stabiliser TS7270 stabilises the output voltage at 5v6.

Switch-on pulse

At switch-on, the voltage across R3272 is lower than 0.7 volts. Transistor TS7273 is not conducting. If the +5-volt stand-by voltage is turned on, the POR signal is kept high via R3274. If the voltage across R3272 increases, TS7273 and thus also TS7272 start conducting and the POR signal is switched to a lower level by TS7272. Meanwhile the power supply has been started and a reset pulse has been supplied to the microcomputer.

8. PIP

Contents

8.1 Introduction

PIP is the abbreviation for Picture In Picture. This is a second picture, reduced, with limited picture sharpness, projected in the large picture. In order to look at another programme in this small picture, the PIP module may be equipped with an extra tuner (otherwise at least one other external source must be connected).
The source which is made visible in the small picture gives no sound information. The sound information always comes from the large picture.

PIP dimensions

A choice can be made between two formats of the PIP picture (1/9 or 1/16 of the main picture). Depending on this, the PIP picture contains more or fewer lines.

PIP framework

There is a frame around the PIP picture. The frame thickness above and below is equal to 4 lines. The frame thickness on the left and right is equal to 0.5μs.

Picture reduction

Only a limited part of the total video signal supplied is used for the PIP acquisition, namely 264 lines, and 47 μs of each line.
The picture is reduced linearly 3 times (4 times with large 1/16). This picture reduction is obtained by averaging picture lines and picture elements. See also section 8.7.

8.2 The block diagram

In the PIPSELECT part (A) it is determined which signal is shown in the PIP picture; this part is on the small signal panel

The PIP CVBS signal selected goes to the PIP panel. There is a second (PIP)tuner/intermediate frequency part on this that can be tuned separately to a transmitter. Here the selection also takes place between the signal of the small signal panel and the signal of the PIP tuner.

The CVBS signal is supplied to the luminance-chrominance part (B) and to the synchronisation part (C). The chrominance signal is separated from the luminance signal and then demodulated, after which both the chrominance and the luminance signal are converted from analog to digital in the D/A converter (D).
Depending on the PIP size selected, the digitised signals are then reduced by a factor of 1:16 or 1:9 and stored in the memory of the PIP processor (E).

Because the second signal source is not synchronous with the main signal source, the signal processing described should by synchronous with the main picture. In order to achieve this, a separate synchronisation part (C) is added which supplies signals which are synchronised with the PIP input signal.

The digital Y, U and V signals stored in the memory are read out and converted to R, G and B signals. In order to obtain a stable PIP picture within the main picture, this must be read out synchronised with the synchronisation signals of the main picture. This synchronisation is obtained by controlling the PLL (F), which activates the read-out clock, with the horizontal synchronisation signal of the main picture.
A PIP fast-blanking signal (FBL PIP) is also controlled by the R, G, B signals if a signal is present from the PIP processor which produces switching between EXT RGB (from EXT1) and PIP RGB.
The RGB output signals, coming from the PIP module, are supplied to the IC7309 (see section 5.5).

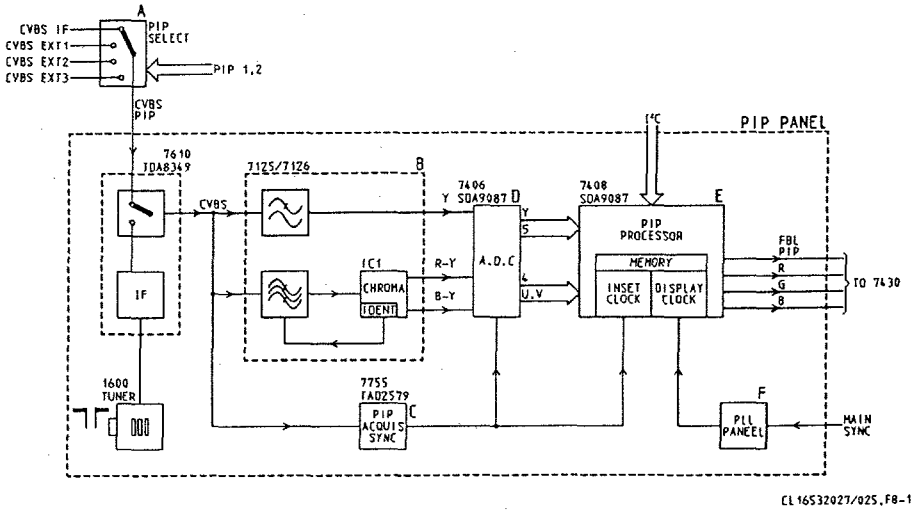


Fig. 8.1

8.3 PIP tuner and source selection

The PIP tuner part consists of tuner UV916, intermediate frequency and demodulation IC TDA8349 and control IC SAA1300.

The tuner

The tuner can receive channels on the VHF1, VHF3, UHF, S and the Hyperband. Internally the tuner is divided over three bands (low band, mid band and high band).
The band selection and tuning frequency required are passed to the channel selector by the control system via the I^2C bus (pins 13 and 14). The channel selector contains a PLL circuit (Phase Locked Loop) which carries out the tuning. The tuner AGC (Automatic Amplifier Control) is controlled at pin 5. The intermediate frequency signal is available at pins 16 and 17.

The IF circuit

The IF signal of the tuner part goes via intermediate frequency filter 1610 to pins 1 and 2 of the intermediate frequency IC7610 (TDA8349). Here the signal first comes to the AGC (Automatic Amplification Control). The AGC controls the signal at the correct level, if necessary with the tuner AGC via pin 4. The video demodulator then demodulates the IF video spectrum at 38.9 MHz with the reference circuit at pins 15 and 16. The required system can be selected via pin 20. The CVBS signal generated in this way is supplied directly to output pin 11. The signal then goes to pin 12. This is one of the inputs of a selector switch. The CVBS signal selected on the small signal panel is supplied to the other input. One of these signals is selected via pin 7. The signal selected is sent for further PIP processing.

The control

IC7630 (SAA1300) contains an I^2C control circuit that controls two outputs in this application:

Pin 3 — This controls the system selection in IC7610. This is done with two levels:
- OV PAL/SECAM BG, NTSC M
- 5V SECAM L

pin 4 — This controls the selector switch.
- OV CVBS of the PIP tuner
- 12V CVBS of the small signal panel

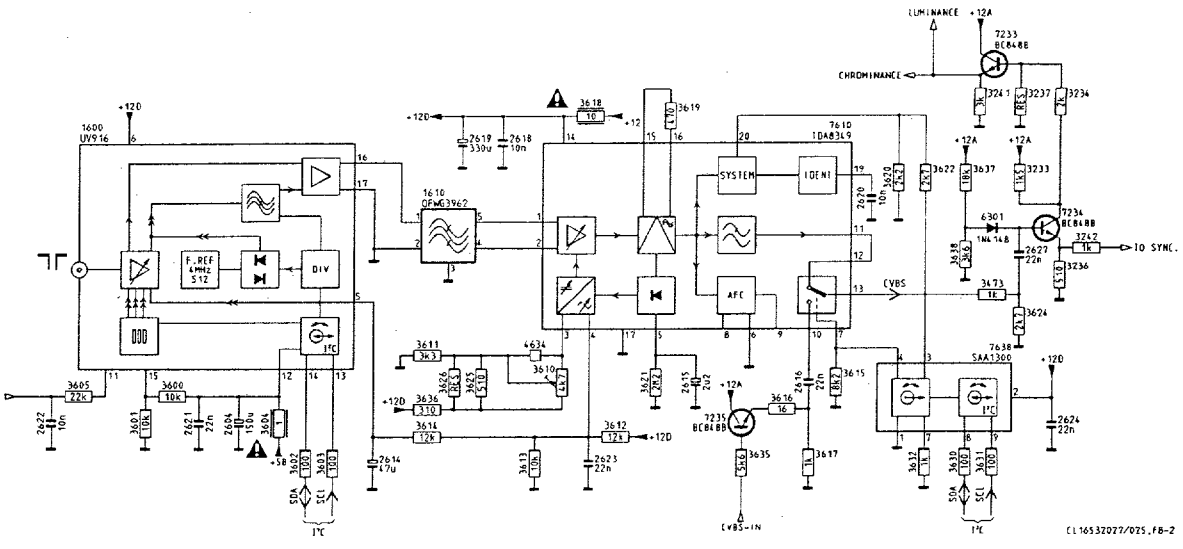


Fig. 8.2

8.4 PIP Chrominance/luminance path

The PIP-CVBS signal comes in on the basis of TS7234 (see fig. 8.3). The emitter signal branches off and goes to the PIP synchronisation IC (IC7755). The amplified signal present on the emitter of TS7233 is separated into a luminance and a chrominance signal.
The luminance signal goes to the ADC SDA9087 (IC7406) after a lowpass filter.
In the case of a single-system unit, the chrominance signal goes to the PAL decoder IC7126. In the case of multi-system units, the chrominance signal is sent to the multi-standard decoder IC7125.

PAL only PIP

The chrominance signal is supplied to pin 9 of IC7126 (TDA4510) via a bandpass filter.
Colour demodulation takes place in this IC. For further information on the operation of this IC , see section 5.4.

Multi-system PIP

In the case of multi-system PIP, the chrominance signal is supplied to pin 15 of IC7125 (TDA4554) via a bandpass filter. The filter can be switched and has 3 positions:

-SECAM — In the SECAM position pins 25, 26 and 28 of IC7125 are low. The input filter now fulfils the circuit clock required for SECAM.

-PAL — Pin 28 of IC7125 is now high, the filter is now tuned to 4.43 MHz.

-NTSC — The filter is now tuned to 3.58 MHz.

System identification

IC7125 (TDA4554) automatically switches one of the colour systems on and checks at the same time pins 25 to 28 for the switching of the input filter. The systems are recognised by the burst or identification signal on the back porch.
The identification recognises these signals and then makes one of the output points 25 to 28 high.
Pin 23 is earthed, which means that SECAM line identification is used.

The colour difference signals B-Y and R-Y from the demodulator (IC7125 or IC7126) are supplied to pins 18 and 17 of the A/D converter, respectively.

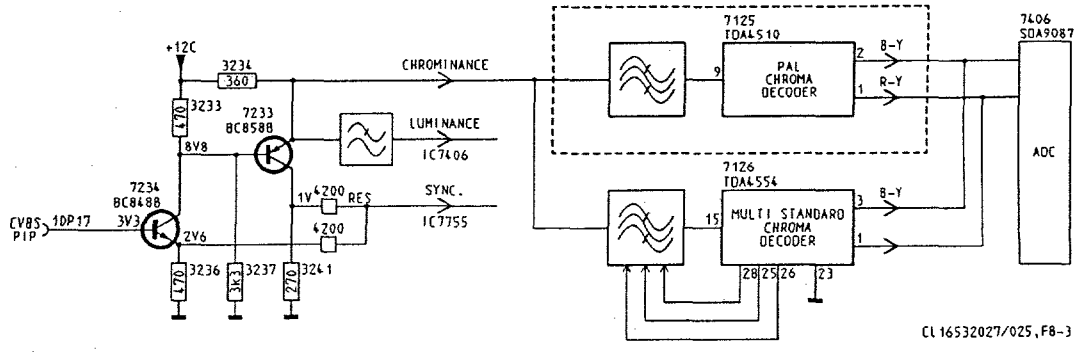


Fig. 8.3

8.5 PIP Synchronisation

Two synchronisations are necessary to process a PIP picture: (see fig. 8.4)

Acquisition Synchronisation

After processing the PIP picture selected is stored in a memory in the PIP processor (IC7408). Synchronisation with the PIP picture is necessary for this. For this a separate synchronisation IC (TDA2579A) is used. This so-called acquisition synchronisation is used in:

- the chrominance part, where the burst key pulse is used to separate burst and chrominance;
- the analog-to-digital converter (A.D.C.), where the burst key is used for clamping, and where a 13.5 MHz clock is produced which is synchronised with the burst key pulse;
- the PIP processor, where the READIN clock is activated which is controlled by the horizontal synchronisation and the 13.5 MHz clock of the A.D.C. and by the vertical synchronisation pulses from the acquisition sync. IC.

Display synchronisation

The display of the PIP on the screen must be synchronised with the main picture. The signals for the reading out of the memory of the PIP processor are therefore synchronised with the horizontal and vertical synchronisation pulses of the main picture (display sync).

Aquisition synchronisation IC (TDA2579)

The CVBS PIP comes in at point 5 of IC7755 (see fig. 8.5). The horizontal oscillator is built up around the C2238, R3238 and R3239 connected to pin 15. Capacitor C2238 is charged with a constant current from the IC7755 to 6 volts and then discharged via R3238 and R3239. By varying the value of R3239, the discharge time, and thus the frequency, can be varied. In order to set the free-running frequency, the input signal can be short-circuited at point 5. The oscillator is now free and this frequency can be adjusted until the picture is still with R3239.

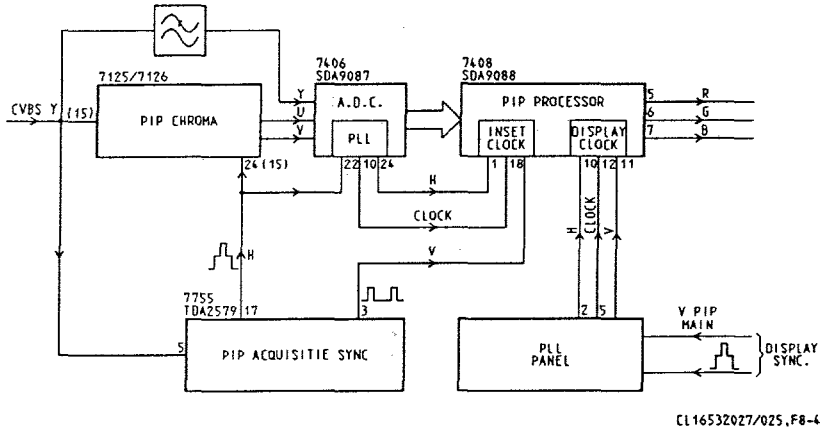


Fig. 8.4

Vertical synchronisation

The vertical synchronisation pulses (V) come to the outside via point 3 and are sent to the PIP processor.

Sandcastle generator

The line pulses supplied by the oscillator (G) go to the sandcastle generator via an amplifier.
The sandcastle pulse at point 17 has two levels:

- 12 volts during the line flyback
- 2.5 volts during the frame flyback

Because the PIP synchronisation does not control any line output stage, the supply voltage (point 10) and the start voltage (point 16) may be switched on at the same time.

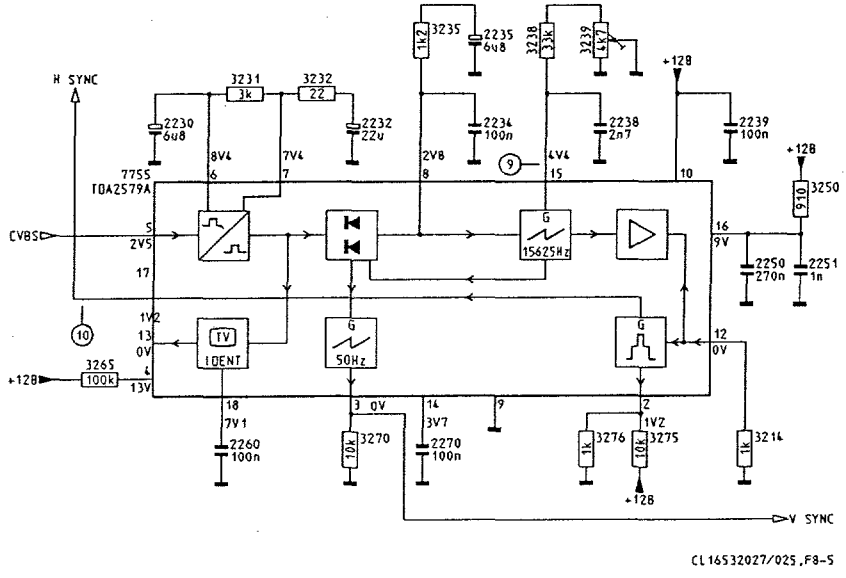


Fig. 8.5

Display synchronisation IC

Display synchronisation for FL1.1 (SDA9086)

The sandcastle of the main picture comes via a difference amplifier (see fig. 8.6) and an emitter follower at point 8 of IC7410. This IC contains a VCO which produces 27 MHz. The clock (27 MHz) is generated by a PLL circuit which is synchronous with the sandcastle of the main picture and is present at pin 5.
The horizontal synchronisation pulse (H) is obtained from the clock (27 MHz/864) and is thus also synchronised with the sandcastle of the main picture.
The PLL compares the divided clock frequency with the signal at point 8, and generates up/down pulses which are smoothed by the RC network at pin 3. Using this the VCO is adjusted until the clock is an exact multiple of the line frequency of the main picture.

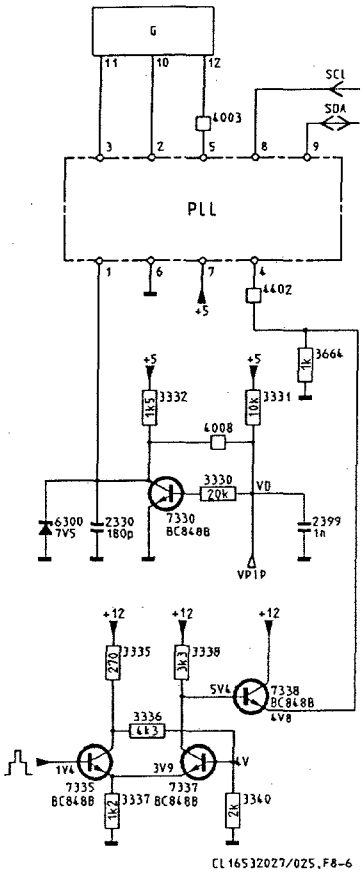


Fig. 8.6

Display synchronisation for FL1.2
Because with chassis FL1.2 the PIP picture must be able to reproduce both 16:9 and 4:3, pictures in 4:3, 16:9 and expand mode of the main picture, various clock frequencies must be available. In order to achieve this, the display synchronisation has several modes. These modes are produced on the PLL panel and controlled via the I^2C bus. The display synchronisation is controlled by the sandcastle of the main picture (13250 Hz). This goes via TS7335, TS7337 and TS7338 to pin 4 of this panel. On the PLL a clock signal is then generated which is synchronised with the sandcastle. The frequency of the signal generated depends on the aspect ratios of the main picture and the PIP picture. The frequency for normal picture reproduction is 27 MHz; however, in the following two modes a different frequency is required:

Frequency	PIP-picture	Main picture
20,25 MHz	16:9	Expand
36 MHz	4:3	4:3/16:9

This frequency change alone is not sufficient to achieve the required result. Via the I^2C bus the time constants are also switched in the PIP processor (IC7408/SDA9088).
The vertical synchronisation is obtained from the VPIP signal. This goes via TS7330 to pin 1 of the PLL panel. This signal is inverted on the PLL panel, after which it goes to pin 11 of IC7408.

8.6 De A/D converter

Internal clock frequency

The analog-to-digital converter is controlled by an internally produced 13.5 MHz clock frequency (see fig. 8.7). This clock frequency is locked to the clock signal supplied to pin 22 from the display sync IC7410.
The colour difference signals R-Y and B-Y enter the A/D converter via TS7402 and TS7400 via pins 17 and 18, respectively.

The Y signal first goes through a lowpass filter to filter out the chrominance signal and to prevent folding deformation.

Reduced bandwidth

Because the signal still ultimately appears in the PIP picture on the screen with a reduced bandwidth, the filter has a tilting point of only 1.3 MHz.

The reference voltages are determined in IC7406 by voltage dividers between pin 13 (Vref Low) and pin 12 (Vref High).

Colour difference signals multiplexed

Because the bandwidth of the R-Y signal and the B-Y signal is smaller than that of the Y-signal, the sample frequency for R-Y and B-Y may be lower than 13.5 MHz.
Thus, the colour difference signals are multiplexed from 5-bit signals with a sample frequency of 13.5 MHz to 2-bit signals with a sample frequency of 13.5 MHz. This takes place by using only one of each of the 4 samples and dividing the 5 bits of this sample over 2 bits and 4 clock periods.
Because the signals are delayed by this (and by the later demultiplexing), the Y-signal must also be delayed.

Luminance delay

This extra delay takes place by an internal delay line, the delay of which is set by the voltage at pins 20 and 21. With the setting used the delay time is set at 6 clock periods. A horizontal blanking pulse is obtained from the digital Y-signal, which is passed on to the PIP processor via pin 24, where this pulse is used to synchronise the read-in clock.

The A.D.C. thus supplies a 5-bit Y-signal, a 2-bits B-Y signal and a 2-bit R-Y signal to the PIP processor.

Y: 5 bits
R-Y : 2 bits
B-Y : 2 bits

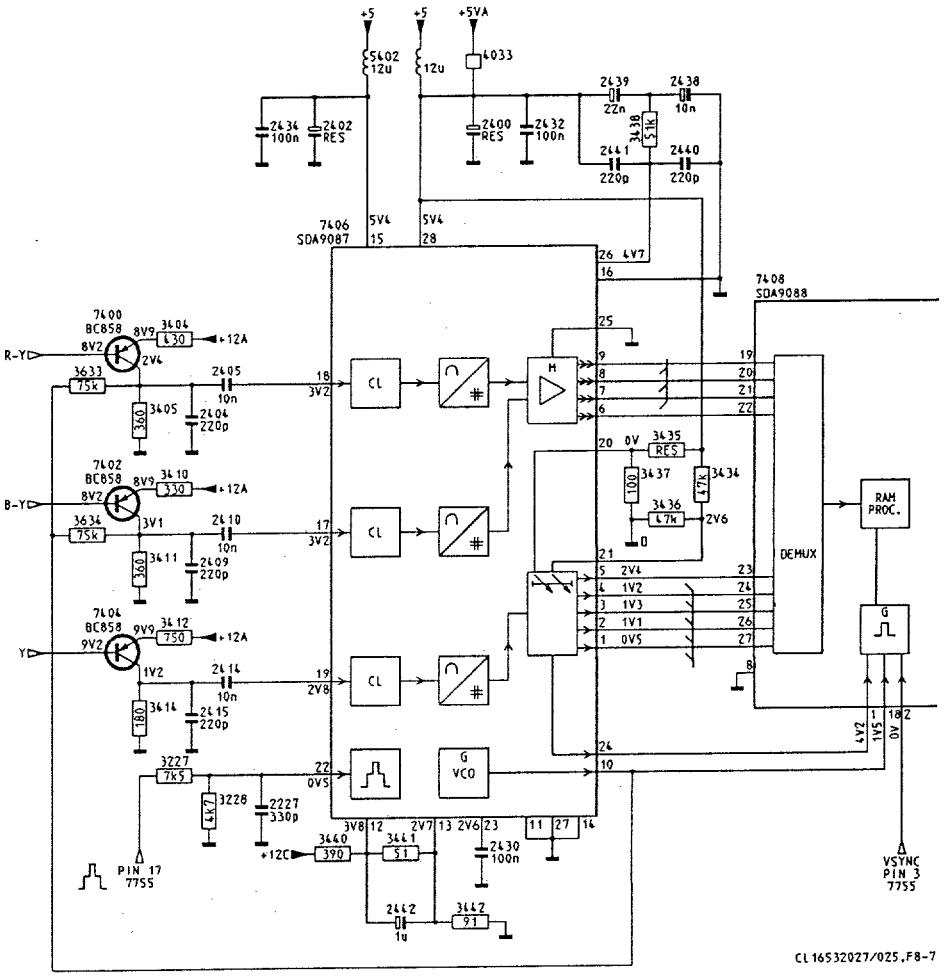


Fig. 8.7

8.7 The PIP processor

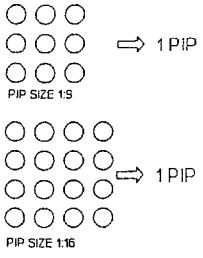


Fig. 8.8

The PIP processor receives one 5-bit Y and two 2-bits (U and V). These colour difference signals are demultiplexed first.

In order to place the PIP picture on a reduced format within the main picture, it must first be compressed. Depending on the PIP size selected, the average of 9 or 16 samples is determined in the decimation filter. This reduction always takes place with 3 or 4 samples in both the horizontal and vertical direction (see fig. 8.8).

In addition to this compression, several lines are left off on the top and bottom of the picture. A number of samples are also left off per line on the left and right. The remaining number of lines and samples is given in table 1.

PIP SIZE	NUMBERS OF PIXELS PER LINE			NUMBER OF LINES
1/9	212	53	53	88
1/116	160	40	40	66

Because the sample frequency for R-Y and B-Y is 4 times lower than for Y, the number of remaining pixels is also 4 times lower.

This reduced information is now stored in the memory using the INSET clock (see section 8.5).
The memory is read using the DISPLAY clock (see also section 8.5).
In order to convert the read-out Y, R-Y and B-Y signals into a matrix, R, G and B signals must have the same sample frequency. The interpolator fulfils this function.

The interpolator

Three intermediate samples are always calculated and inserted in the interpolator by linear interpolation between two consecutive samples of R-Y and B-Y.
Y, R-Y and B-Y now have the same sample frequency (13.5 MHz).

In the PIP frame blanking part a pulse is produced which is high during the presence of the PIP picture. This fast blanking is carried out via pin 9 and is used to blank the main picture when the PIP picture is present.

The RGB matrix

R-Y, B-Y and Y are converted into R, G and B in the matrix.

The DA converter

In the digital-to-analog converter the digital R, G and B signals are converted into analog signals which are then carried out via pins 5, 6 and 7.

EXT RGB / PIP RGB

In IC7380 a selection is made between RGB from EXT1 or RGB PIP using the PIP frame blanking signal.

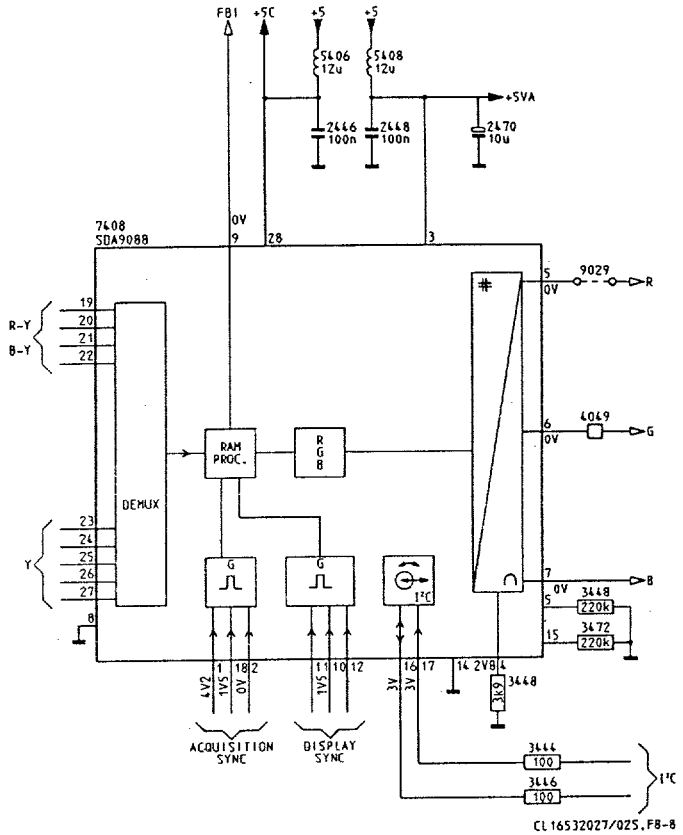

FB1
+5C
+5
+5
5406
12u
5408
12u
+5VA
2446
100n
2448
100n
2470
10u
7408
SDA9088
0V
9
28
3
5
0V
9029
R
R-Y
B-Y
19
20
21
22
RAM
PROC.
R
G
B
DEMUX
6
0V
4049
G
Y
23
24
25
26
27
8
G
G
I²C
7
0V
B
5
3448
220k
15
3472
220k
1
18
2
11
10
12
16
17
14
2V8
4
3448
3K9
4V2
1V5
0V
1V5
3V
ACQUISITION
SYNC
DISPLAY
SYNC
3444
100
3446
100
I²C
CL16532027/025.F8-8

Fig. 8.9